2014 S2L55m Chip Datasheet - Preliminary

SUMMARY DESCRIPTION

The S2L55m is an integrated system-on-a-chip (SoC) platform that targets IP cameras for advanced consumer/cloud 3Mp30 surveillance applications with HDR support.

S2L55m chips provide a 600-MHz ARM Cortex-A9 CPU and a high-performance digital signal processing (DSP) subsystem with an image sensor pipeline (ISP) and a high-definition (HD) H.264 codec engine.

KEY FEATURES

- Embedded ARM Cortex-A9 600-MHz CPU with L2 cache
- More than 240 MPixel/s processing rate
  - 5-MPixel maximum sensor resolution
- Lens distortion correction for wide-angle lenses
- Wide Dynamic Range (WDR) image processing
- High Dynamic Range (HDR) engine with multi-exposure fusion
- 3D noise reduction (Motion Compensated Temporal Filter, or MCTF)
- H.264 BP/MP/HP Level 4.1 and MJPEG codecs
- Maximum encode resolution: 5 Mpixels
- Support for Ambarella SmartAVC low bitrate streaming
- 256-pin, 0.65-pitch TFBGA package (11 mm x 11 mm)
- 28-nm CMOS Low Power (LP) technology
- Operating temperature from 0 C to 70 C

CONTENTS

1. OVERVIEW

This preliminary datasheet for the S2L55m processor from Ambarella begins with a brief introduction to the chip (Section 1.1) and a summary of key features (Section 1.2). Chapter 2 describes the S2L55m peripheral interfaces. For pin details and electrical characteristics refer to Chapter 3 and Chapter 4, respectively. See Chapter 5 for package information and Chapter 6 for Ambarella contact and ordering details.

Please note that the chip features described in this datasheet are subject to change. Details that have not been entirely finalized (e.g., encoding specifics) are provided using conservative estimates (i.e., final encoding performance is expected to meet or exceed the estimate provided). Please contact an Ambarella representative for additional information.

1.1 Introduction

The S2L55m is an integrated system-on-a-chip (SoC) platform that targets IP cameras for advanced consumer/cloud 3Mp30 surveillance applications with HDR support, including telco operator applications and cloud storage services for residential-level applications. S2L55m chips provide a single-core Cortex-A9 ARM CPU and a high-performance digital signal processing (DSP) subsystem with an image sensor pipeline (ISP) and a high-definition (HD) H.264 codec engine. A functional block diagram of the S2L55m SoC is provided below.

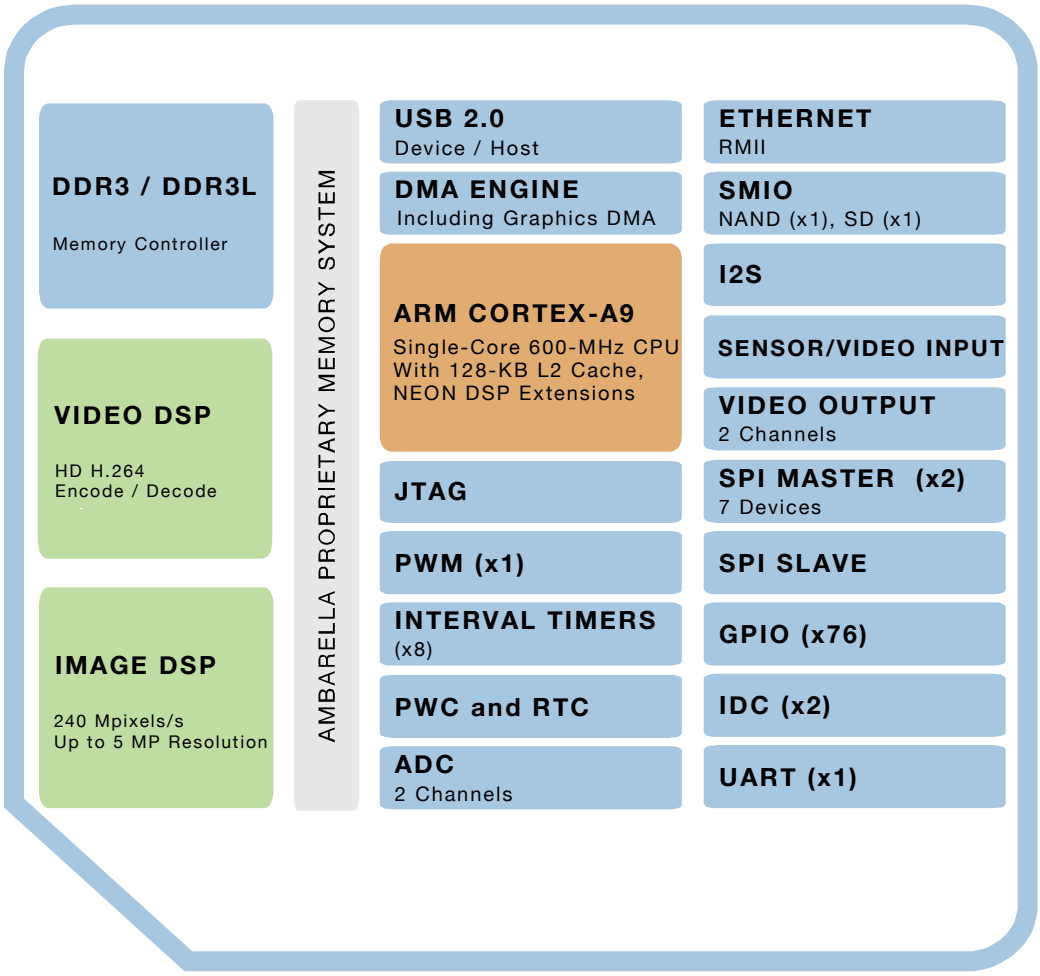


Figure 1-1. S2L55m Overview: Functional Block Diagram of the S2L55m SoC.

The S2L55m SoC provides a glueless interface to Serial SLVS, HiSPi, and MIPI interfaces, as well as parallel connections to popular CMOS image sensors. The ISP offers advanced image-processing features including improved high dynamic range (HDR) processing with multi-exposure fusion, wide dynamic range (WDR) single-exposure tone mapping with local contrast enhancement, 3D noise reduction (Motion Compensated Temporal Filter, or MCTF), and geometric lens correction (for wide-angle lenses).

The H.264 codec engine delivers versatile encoding up to 3Mp30 total performance, including up to four simultaneous encode streams and support for up to 5 MP H.264 and 5 MP JPEG. The high-efficiency H.264 encoder supports SmartAVC, as well as advanced Main and High-Profile functions for the highest-quality and lowest possible bitrate. These functions include bidirectional prediction (B-frames), large motion-estimation search range, and macroblock-level quantization. Ambarella builds in flexibility with a multi-streaming function (up to four streams), allowing on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream.

A 600-MHz ARM Cortex-A9 CPU with NEON DSP extensions and floating point support is available for implementing full-featured user applications.

The S2L family is fabricated using low-power 28-nm CMOS technology and integrates advanced power-saving modes, such as utilizing DSP-subsystem memory resources to reduce external memory bandwidth and total camera system power requirements. The S2L evaluation kit (EVK) and software development kit (SDK) provide a Linux-based framework and development environment that includes demonstration applications, source code, image-tuning tools, and a rich set of APIs that expose the DSP imaging and codec functionality at the ARM level, enabling a range of product customization and differentiation options.

1.2 Feature List

Features of the S2L55m chip include:

- Embedded ARM single-core Cortex-A9 CPU
  - Clock frequency up to 600 MHz
  - 32-KByte data / 32-KByte instruction cache
  - 128-KByte L2 cache
  - NEON SIMD engine
  - Floating Point Unit (FPU)
  - AES/3/DES/SHA-1/MD5 encryption engine
- DDR3 and DDR3L controller
  - Up to 528-MHz clock rate
  - 16-bit wide data bus
  - Maximum capacity of 2 Gbits (256 MBytes)
- Image pipeline
  - More than 240 MPixel/s processing rate
  - 5-MPixel maximum sensor resolution
  - Geometric lens correction (for wide-angle lenses)
  - Black level correction

- Dynamic and static defect pixel cluster correction
- RGB Bayer demosaicing
- Lens shading correction
- 3D LUT color transform with gamma
- Wide Dynamic Range (WDR) single-exposure tone mapping
- High Dynamic Range (HDR) engine with multi-exposure fusion
- 3D noise reduction (Motion Compensated Temporal Filter, or MCTF)
- Flexible APIs and image-tuning tools
- Adjustable 3A; exposure, white balance and focus control (AE/AWB/AF)
- RGB and YUV statistics, histogram and AF focus value generation
- Luma sharpen and chroma noise filter
- Four resizers (1/16x to 8192x scaling) with digital pan, tilt and zoom (PTZ)
- Crop, mirror, flip, 90°/270° rotation
- Alpha-blending OSD up to full-frame overlay for text, image and privacy mask

• Video engine

- Maximum encode resolution: 2592x1944
- H.264 BP/MP/HP Level 4.1 and MJPEG codecs
- Encode performance up to 3Mp30 with four flexible streams
  - Up to four real-time simultaneous encodes with on-the-fly start/stop as well as the adjustment of the bitrate, frame rate, and GOP of each individual stream
- Advanced H.264 compression tools
  - I, IP, IBP modes (M=1,2,3; IP, IBP, IBBP)
  - SVCT Scalable Video Coding
- Flexible rate control
  - SmartAVC ultra-low bitrate H.264 streaming
  - CBR, VBR and Constant QP with max bitrate control
  - Macroblock-level adaptive quantization
- Dynamic ROI encoding with unrestricted number of free-form areas at macroblock boundary

• Sensor/Video Input (VIN) interface

- Multiple input modes
  - Supports up to 8-lane SLVS / HiSPi input
  - Supports up to 4-lane MIPI input
  - Support for 14-bit parallel and LVCMOS sensors
- Support for popular CMOS sensors; Aptina, Sony, OV, Panasonic
- 16-bit CCIR.601 video input with external sync signals
- 8-bit, 10-bit, 12-bit or 14-bit BT.656 video input with embedded sync codes including full-data-

range support

- Video Output (VOUT) interfaces
  - Two video output ports
    - One logical channel drives analog
    - One logical channel drives digital
  - Popular LCD panel controllers (RGB mode)
  - Support for RGBA and YUVA OSD
  - Video DAC for 480i/576i composite PAL/NTSC output
  - BT.656 embedded sync YUV output (8-bit or 16-bit mode)
- AHB Bus DMA controller
  - Memory-to-memory transfers including support for transfers between memory and peripherals
  - Programmable transfer count up to 4 MB
  - DMA scatter/gather via chained descriptor list in memory with DMA control information source
- Dedicated DMA co-processor for graphics and image operations
  - Offers linear copy, 2-D copy, composite, and alpha-blend image operations
  - Supports 4- to 32-bit pixel formats
- I2S digital audio interface (stereo)
  - Audio record/playback
- Ethernet MAC controller
  - IEEE 802.3 compliant with full- and half-duplex (IEEE 802.3x flow-control) and Jumbo frames
  - IEEE 802.1Q VLAN tag detection
  - Checksum off-load for received IP and TCP/UDP packets
  - Dedicated pins for RMII or MII interface
  - FIFO (2 KB / 2 KB) and DMA support
- One USB 2.0 interface
  - One port configurable as host or device, with built-in PHY
- Flexible Storage Media Input / Output (SMIO) interface
  - NAND Flash controller
    - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes
    - 8-bit flash chip data bus
    - 4-bit and 8-bit SLC with ECC hardware and read-confirm support
    - BCH error correction and increased spare area available
  - One SD controller (SD0)
    - 1-bit, 4-bit SD modes, CRC7 for command and CRC16 for data integrity
- Multiple boot options

  - SPI-NOR, NAND Flash, USB and eMMC
- Vector interrupt controller including VIC CPU-offload functionality
- SSI / SPI controller interfaces
  - Two SSI / SPI masters with up to seven device enables
  - One dedicated SSI / SPI slave port to connect to an external system master
- Two-wire serial Inter-Integrated Circuit (IDC) interfaces (x2)
  - Configurable IDC buses
- UART interfaces (x2)
- Up to 76 General Purpose Input/Output (GPIO) short-height pins with individual pull-up/down control
- ADC (two channels) with high/low threshold interrupt generation and 12-bit resolution
- Built-in power controller for power-up/down sequencing
- Real Time Clock (RTC)
- Interval timing with eight general-purpose timers configurable as external event counters
- Watchdog timer (one)
- One Pulse Width Modulator (PWM)
- JTAG In-Circuit Emulator (ICE) interface for debugging (one)
- 256-pin, 0.65-pitch TFBGA package (11 mm x 11 mm)
- 28-nm CMOS Low Power (LP) technology
- Operating temperature from 0 C to 70 C

2. INTERFACES

2.1 Overview

This section summarizes the peripheral interfaces for the S2L55m chip as follows:

2.2 SDRAM Interface

The S2L55m chip includes a synchronous DRAM interface, enabling high data-access rates in response to pipe-lined commands. The features of the S2L55m SDRAM interface include:

- Frequencies up to 528 MHz
- Support for DDR3 and DDR3L operations
- Programmable I/O strength
- 16-bit data bus

Please contact an Ambarella representative to select a qualified Ambarella-approved DDR component.

2.3 Video Input (VIN) Interface

The S2L55m chip supports multiple serial and parallel input modes. The features of the S2L55m VIN interface include:

- Up to 8-lane SLVS / HiSPi input
- Up to 4-lane Camera Serial Interface (CSI) MIPI input
- Support for 14-bit parallel and LVCMOS sensors
- 16-bit CCIR.601 video input with external sync signals
- 8-bit, 10-bit, 12-bit or 14-bit BT.656 video input with embedded sync codes including full-data-range support

The following table summarizes the S2L55m-supported input data formats, as well as their associated data ports and link types/speeds.

Data Format	Link Type/Speed	Port Selection
YUV (YCbCr)	> 74.25 MHz ≤ 150 MHz	External LVCMOS YUV (YCbCr)
Sensor Data	LVCMOS ≤ 150 MHz	Parallel LVCMOS
Sensor Data	SLVS ≤ 700 Mbps	Serial SLVS
Sensor Data	MIPI ≤ 1 Gbps	Serial MIPI CSI

Table 2-1. Video Input Port Selection.

The S2L55m VIN module is part of the DSP cluster. Like other modules in the DSP cluster it is configured using a set of APIs. Please contact an Ambarella representative for information regarding VIN module configuration for a specific sensor.

2.3.1 Input Modes

The S2L55m chip supports the following input modes:

- (Section 2.3.1.1) Input Mode: External YUV Source
- (Section 2.3.1.2) Input Mode: Bayer Data Parallel Input LVCMOS
- (Section 2.3.1.3) Input Mode: Serial SLVS
- (Section 2.3.1.4) Input Mode: MIPI Camera Serial Interface (CSI)

2.3.1.1 Input Mode: External YUV Source

- Port: External LVCMOS YUV
- Pixel clock: **SPCLK_LVDS_P_0**
- Pixel data [7:0]: **SD_LVDS_P_[7:0]** (8-bit and 16-bit modes)
- Pixel data [15:8]: **SD_LVDS_N_[7:0]** (16-bit mode)
- HSync: **SPCLK_LVDS_N_0**
- VSync: **SPCLK_LVDS_N_1**
- SField: **SPCLK_LVDS_P_1**

2.3.1.2 Input Mode: Bayer Data Parallel Input LVCMOS

- Port: Parallel LVCMOS
- Pixel clock: **SPCLK_LVDS_P_0**
- Pixel data [7:0] (single-ended): **SD_LVDS_P_[7:0]**
- Pixel data [13:8] (single-ended): **SD_LVDS_N_[5:0]**
- HSync: **SPCLK_LVDS_N_0** (Slave Mode - Input is received from the video / sensor device)
  SHSYNC (Master Mode - the S2L55m video input unit drives the sync operation)
- VSync: **SPCLK_LVDS_N_1** (Slave Mode)
  SVSYNC (Master Mode)
- SField: **SPCLK_LVDS_P_1**

2.3.1.3 Input Mode: Serial SLVS

- Port: Serial SLVS
- For every four serial lanes, there should be one sync clock
- Includes support for one, two, four, or eight serial lanes
- Connect the input clock to **SPCLK_LVDS_P/N_[1:0]** as described in the table below.
- Connect the input data to **SD_LVDS_P/N_[7:0]** as described in the table below
- If only one clock is used then connect it to **SPCLK_LVDS_P/N_0**

Number of Data Lanes Used	Mapping	
	Clock	Data Lanes
2	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[1:0]**
4	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[3:0]**
8 (except as below*)	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[3:0]**
	SPCLK_LVDS_P/N_1	**SD_LVDS_P/N_[7:4]**
*Sensors with only one CLK	**SPCLK_LVDS_P/N_0**	**SD_LVDS_P/N_[7:0]**

Table 2-2. SLVS: Sensor Input Port Clock Mapping for the SLVS Interface.

2.3.1.4 Input Mode: MIPI Camera Serial Interface (CSI)

- Port: Serial MIPI CSI
- Capability: Up to 4-lane MIPI CSI interface to compatible sensors
- Data Formats: Raw-8, Raw-10, Raw-12, Raw-14, YUV-422-8, and Generic-8
- Connect clock to **SPCLK_LVDS_P/N_0**
- Connect data lanes to **SD_LVDS_P/N_[3:0]**

2.4 Video Output (VOUT) Interfaces

The S2L55m Video Output (VOUT) interface supports a total of two output ports.

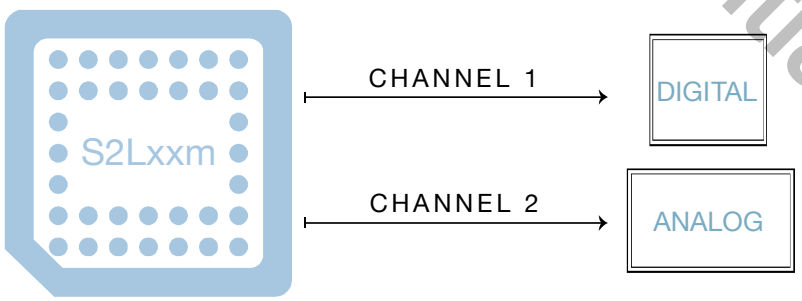


Figure 2-1. S2L55m Video Output Channels and Ports.

One VOUT channel is capable of driving digital output to RGB format, while the second VOUT channel drives analog composite output. The S2L55m chip supports simultaneous 1080i and 480i output rates.

2.4.1 Analog Video Output

The S2L55m video digital-to-analog converter (DAC) can drive standard-definition 480i/576i composite video outputs. Refer to the "*S2L Hardware Programming Reference Manual*" for VOUT register programming details.

2.4.2 Digital Video Output

The S2L55m chip supports several digital video output modes including 16-bit RGB and BT.656 as described in the tables below.

Refer to the "*S2L Hardware Programming Reference Manual*" for VOUT register programming information.

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved R,G,B	**VD0_OUT[7]** is MSB

Table 2-3. Digital RGB Mode (Video Output Modes 0/1/2 for 3-bit Output).

Bits	Mapped To Signal	Notes
VD0_OUT[15:11]	Upper 5 bits of the Red channel	**VD0_OUT[15]** is the MSB
VD0_OUT[10:5]	Upper 6 bits of the Green channel	**VD0_OUT[10]** is the MSB
VD0_OUT[4:0]	Upper 5 bits of the Blue channel	**VD0_OUT[4]** is the MSB

Table 2-4. 5:6:5 RGB Mode (Video Output Mode 3 for 16-bit RGB Output).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Unused	
VD0_OUT[7:0]	Interleaved Cb,Y,Cr,Y . . .	Output data rate is 13.5 MHz Clock rate is 27 MHz

Table 2-5. 656 YCbCr Mode (Video Output Mode 4 for D1 - 480i and 576 - Resolution).

Bits	Mapped To Signal	Notes
VD0_OUT[15:8]	Interleaved Cb,Cr	**VD0_OUT[15]** is the MSB
VD0_OUT[7:0]	Y	**VD0_OUT[7]** is the MSB

Table 2-6. 16-bit 656-YCbCr Mode (Video Output Mode 4) and 16-bit 601-YCbCr Mode (Video Output Mode 5).

Table 2-5 and Table 2-6 correspond to 4:2:2 output format.

2.4.3 Supported Video Format Per Output Port

Video formats for the each of the S2L55m video output ports are summarized in the table below.

Video Format Output		Analog Composite	HDMI	Digital Video	Comments
SD	720x480i59.94	√	x	√	
	720x480i60	√	x	√	
	720x576i50	√	x	√	
	720x480p30/29.97	x	x	√	
ED	720x480p59.94	x	x	√	
	720x480p60	x	x	√	
	720x576p50	x	x	√	
HD	1280x720p25	x	x	√	
	1280x720p30	x	x	√	
	1280x720p50	x	x	√	
	1280x720p59.94	x	x	√	
	1280x720p60	x	x	√	
	1920x1080p24	x	x	√	
	1920x1080p25	x	x	√	
	1920x1080p30	x	x	√	
	1920x1080p50	x	x	√	
	1920x1080i59.94	x	x	√	
	1920x1080i60	x	x	√	
	1920x1080p60	x	x	√	

Table 2-7. Summary of Video Formats for Each Output Port; Where √ = Supported and x = Not Supported.

2.5 I2S Audio Interface

The S2L55m chip provides an Integrated Interchip Sound (I2S) controller for two-channel audio support. Features of the I2S interface include:

- Support for audio using an external audio codec
- I2S host interface support

Refer to the "*S2L Hardware Programming Reference Manual*" for I2S register programming details.

2.6 Ethernet Interface

The S2L55m Ethernet interface enables a host to transmit and receive data in compliance with the "*IEEE 802.3-2002 Standard for Ethernet Based LANs".* Features include:

- Supports 10/100-Mbps data transfer rates with IEEE 802.3-compliant RMII and MII interfaces to communicate with an external Fast Ethernet PHY

- Supports both full-duplex and half-duplex operation
- MDIO Master interface (optional) for PHY device configuration and management
- A second 25-MHz clock pin for Ethernet PHY

2.7 USB Interfaces

The S2L55m SoC includes one USB 2.0 high-speed interface. Features of the S2L55m USB interface include:

- One configurable USB host/device with a built-in PHY
- USB power-on boot mode

Refer to the "*S2L Hardware Programming Reference Manual*" for USB register programming information.

2.8 Smart Media Input/Output (SMIO) Interface

The S2L55m chip provides Smart Media Input/Output (SMIO) pins as a flexible storage-media interface for NAND Flash and SD controllers. Features of the S2L55m SMIO interface include:

- NAND Flash controller
  - Up to 8-Gbit device, 512-Byte and 2-KByte page sizes
  - 8-bit flash chip data bus
  - 4-bit and 8-bit single-level cell (SLC) memory with error-correcting code (ECC) hardware and read-confirm support
    - Note that Ambarella has discovered and addressed a hardware bug inside the SLC NAND controller related to multi-bit ECC status handling. The symptom of this bug is that, during multi-bit ECC SLC NAND DMA operations, the ECC error status bit is occasionally set for data blocks containing no error. The root cause of the bug is that the ECC error status bit becomes sticky once there is any block with an ECC error during any previous transaction. Ambarella offers pure software multi-bit ECC management for SLC NAND flashes that require multi-bit ECC as a complete workaround.
- One SD controller (SD0)
  - 1-bit, 4-bit SD modes, cyclic redundancy check 7 (CRC-7) for command, and cyclic redundancy check 16 (CRC-16) for data integrity
- Power-on NAND Flash and eMMC boot modes

Refer to the "*S2L Hardware Programming Reference Manual*" for SMIO register programming details.

2.9 SSI/SPI Interface

The S2L55m chip provides two Synchronous Serial Interface (SSI) / Serial Peripheral Interface (SPI) masters and one dedicated SSI/SPI slave for full-duplex data transmission support. Features of the S2L55m SSI/SPI interface include:

- SSI/SPI master control of up to seven slave devices
- Dedicated SSI/SPI slave port for connection to an external system master
- SPI-NOR, SPI-EEPROM boot support included

Refer to the "*S2L Hardware Programming Reference Manual*" for SSI/SPI register programming information.

Master	Number of Device Enables	Device Enable Pins	SSI/SPI Function	Default Polarity[1]
SSI0	3	SSIOEN0	ssi0_en0 Device Enable	Active Low
		SSIOEN1	ssi0_en1 Device Enable	Active Low
		TIMER2	ssi0_en3 Device Enable	Active Low
SSI1	4	ENET_RXD_0	ssi1_en0 Device Enable	Active Low
		ENET_RXD_1	ssi1_en1 Device Enable	Active Low
		ENET_RX_ER	ssi1_en2 Device Enable	Active Low
		ENET_CRS_DV	ssi1_en3 Device Enable	Active Low

Table 2-8. S2L55m SSI / SPI Master with Device Enable Detail.

Note:

1. Each SSI / SPI device-enable has programmable polarity; i.e., the polarity can be assigned to meet peripheral requirements without external glue logic.

2.10 IDC Interface

The S2L55m SoC includes two Inter-Integrated Circuit (IDC) interfaces to provide bidirectional data communication between the chip and its peripheral devices. Features of the S2L55m IDC interfaces include:

- Two programmable IDC ports (IDC0 and IDC2)
- Protocol speeds up to 400 Kbps
- Support for single-master mode

Refer to the "*S2L Hardware Programming Reference Manual*" for IDC register programming details.

2.11 UART Interface

The S2L55m chip includes two Universal Asynchronous Receiver / Transmitter (UART) ports. Features of the S2L55m UART interface include:

- Debugging support
- A maximum baud rate of 115.2 Kbps for UART0, based on per-port software settings

Refer to the "*S2L Hardware Programming Reference Manual*" for UART register programming.

2.12 InfraRed Remote Interface

The S2L55m chip provides one InfraRed (IR) receiver interface to enable remote control functionality. The S2L55m IR pin receives input signals from the IR module, and these signals are decoded through software programming. Refer to the "*S2L Hardware Programming Reference Manual*" for IR register programming information.

2.13 General Purpose Input/Output (GPIO) Interface

The S2L55m SoC includes up to 76 CMOS pins which can be programmed for multi-use General Purpose Input/Output (GPIO) functions. Features of the S2L55m GPIO interface include:

- Multiplexing support, allowing GPIO pins to be assigned multiple functions that can be independently enabled via software
- Individual pull-up/down control
- Individual drive strength control

Refer to the "*S2L Hardware Programming Reference Manual*" for GPIO register programming details.

2.14 Analog-to-Digital Converter (ADC) Interface

The S2L55m chip provides multiple channels for analog-to-digital conversion (ADC). Features of the S2L55m ADC interface include:

- Two channels
- High/low threshold interrupt generation
- 12-bit resolution

Refer to the "*S2L Hardware Programming Reference Manual*" for ADC register programming information.

2.15 Power Controller (PWC) and Real Time Clock (RTC) Interfaces

To conserve power, the S2L55m system software optimizes clock and PLL frequencies according to operating mode. Peripheral clocks can be further optimized by the user through register programming. Refer to the "*S2L Hardware Programming Reference Manual*" for information regarding register programming with peripheral clocks.

Features of the power controller (PWC) and real-time clock (RTC) interfaces include:

- 32-bit embedded RTC maintained with one dedicated always-on power supply pin
- RTC provides current time, alarm set, and power-on and power-off sequence generation

Refer to the "*S2L Hardware Programming Reference Manual*" for PWC/RTC register programming details.

2.16 Pulse Width Modulator (PWM) Interfaces

2.16.1 Pulse Width Modulator (PWM)

The S2L55m chip provides one pulse width modulation interface:

- The S2L55m external pin **VD_PWM** serves as a PWM controller.
- Selection of PWM functions is executed via software.

Refer to the "*S2L Hardware Programming Reference Manual*" for PWM register programming details.

2.17 JTAG Interface

The S2L55m chip provides an interface for JTAG In-Circuit Emulator (ICE) debugging. Contact an Ambarella representative for more information regarding the JTAG interface.

3. PINS

3.1 Pins: Overview

The S2L55m SoC is equipped with 256 external physical pins including power balls, ground balls, and signal balls. This section provides pin details for the primary chip interfaces and functions.

- Refer to Section 4.4 for a list of fail-safe CMOS pins and their corresponding voltage thresholds.
- Refer to Chapter 7 for a complete list of pins sorted by their location on the S2L55m ball map.
- Refer to the "*S2L Hardware Programming Reference Manual*" for GPIO multi-function selection information.

3.2 Pins: Tables

This section lists the pins for each interface as follows:

For each pin listed, the following information is provided:

- Pin direction: (I) input, (O) output, (S) supply, (G) ground
- Pad type
- A brief description
- For complete multiplexing information, please refer to Section 3.2.12 and Chapter 7.

3.2.1 Pins: SDRAM

Name	Location	Dir	Type	Description
DDR_ADDR_[0:13]	E13, E15, F15, C15, E14, D15, D14, C16, D16, F13, E16, F14, E12	O	SSTL	Address for row address strobe (RAS) and column address strobe (CAS)
DDR_BA_[0:2]	G15, F16, G16	O	SSTL	Bank address
DDR_CALIBR	B7	I/O	Analog	DDR3 - ZQ calibration
DDR_CAS	H16	O	SSTL	Column address strobe (active low)
DDR_CK	A16	O	SSTL	DRAM clock per SDRAM
DDR_CK_BAR	B16	O	SSTL	**DDR_CK** and **DDR_CK_BAR** are differential clocks
DDR_CKE	J14	O	SSTL	Clock enable
DDR_DM_[0:1]	D13, A7	O	SSTL	Data write mask (1 bit per 8 data bits)
DDR_DQ_[0:15]	A15, B15, B14, A14, B13, A13, C14, C13, D12, C12, A11, B11, A10, B10, A9, B9	I/O	SSTL	Bi-directional data bus
DDR_DQS_[0:1]	B12, A8	I/O	SSTL	Data strobe (1 bit per 8 data bits) Output with write data, center-aligned Input with read data, edge-aligned
DDR_DQS_BAR_[0:1]	A12, B8	I/O	SSTL	**DDR_DQS_[N]** and **DDR_DQS_BAR_[N]** are differential signals
DDR_ODT	H15	O	SSTL	SDRAM on-die termination control signal
DDR_RAS	G13	O	SSTL	Row address strobe (active low)
DDR_RESET	J15	O	SSTL	DDR3 - Asynchronous reset
DDR_WE	H14	O	SSTL	Write enable (active low)
DDR_VREF	C11	I/O	SSTL	Reference Voltage for SSTL pad (0.5***DDR_VDDQ**)
DDR_VDDQ_[L]	C4, C5, C6, C7, C8, C9, C10, D11	S	Digital Supply	DDR digital I/O power supply

Table 3-1. SDRAM Pins.

3.2.2 Pins: Sensor / Video Input

3.2.2.1 VIN Pins: Sensor Interface

Name	Location	Dir	Type	Description
CLK_SI	J1	I/O	CMOS	Sensor master clock output
SD_LVDS_N_[0:7]	T4, P5, T3, R2, P8, T8, R8, P7	I	SLVS/ LVCMOS /MIPI	Sensor data Differential for SLVS and MIPI Single-ended for LVCMOS mode. Termination resistor built in for SLVS/MIPI mode. Both single and double data rates supported.
SD_LVDS_P_[0:7]	R4, R5, R3, P2, N8, T7, R7, N7	I	SLVS/ LVCMOS /MIPI	
SHSYNC	N10	O	CMOS	H-Sync / H-Valid with Master mode configuration
SPCLK_LVDS_N_[0:1]	T6, J9	I	SLVS/ LVCMOS /MIPI	Sensor pixel clock Differential pairs for SLVS and MIPI modes. **SPCLK_LVDS_P_0** is used for single-ended pixel clock with LVCMOS mode.
SPCLK_LVDS_P_[0:1]	T5, J8	I	SLVS/ LVCMOS /MIPI	
SVSYNC	L10	I/O	CMOS	V-Sync / V-Valid with Master mode configuration
MIPI_VDDIO	T9	S	Analog Supply	VIN PHY digital power. 1.8V for LVCMOS, 1.0V for MIPI

Table 3-2. VIN Sensor Interface Pins.

3.2.3 Pins: Video Output

This section covers video output interface pins for Digital-to-Analog Conversion and Digital Video Output.

3.2.3.1 VOUT Pins: Video Digital-to-Analog Conversion (DAC)

Name	Location	Dir	Type	Description
DAC_COMP	F2	I/O	Analog	Compensation pin
DAC_IO	D1	I/O	Analog	Composite CVBS output
DAC_RSET	F1	I/O	Analog	Reference resistor
DAC_VREFIN	E1	I/O	Analog	Voltage reference input

Table 3-3. Video DAC Pins.

3.2.3.2 VOUT Pins: Digital Video Output

Name	Location	Dir	Type	Description [1]
VD0_CLK	M11	I/O	CMOS	Video output clock
VD0_HSYNC	T13	I/O	CMOS	Video output HSync signal
VD0_HVLD	P14	I/O	CMOS	Video output data
VD0_OUT_0	T15	I/O	CMOS	Video output data
VD0_OUT_1	P11	I/O	CMOS	Video output data
VD0_OUT_2	R11	I/O	CMOS	Video output data
VD0_OUT_3	P10	I/O	CMOS	Video output data
VD0_OUT_4	L9	I/O	CMOS	Video output data
VD0_OUT_5	R13	I/O	CMOS	Video output data
VD0_OUT_6	T16	I/O	CMOS	Video output data
VD0_OUT_7	T14	I/O	CMOS	Video output data
VD0_OUT_8	R12	I/O	CMOS	Video output data
VD0_OUT_9	R14	I/O	CMOS	Video output data
VD0_OUT_10	P12	I/O	CMOS	Video output data
VD0_OUT_11	P13	I/O	CMOS	Video output data
VD0_OUT_12	N11	I/O	CMOS	Video output data
VD0_OUT_13	M9	I/O	CMOS	Video output data
VD0_OUT_14	N12	I/O	CMOS	Video output data
VD0_OUT_15	N13	I/O	CMOS	Video output data
VD0_VSYNC	N9	I/O	CMOS	Video output VSync signal

Table 3-4. Digital Video Output Pins.

Note:

1. S2L55m digital video output pins are used for power-on configuration (POC). For complete POC information, please refer to the "*S2L Hardware Programming Reference Manual*".

3.2.4 Pins: I2S Digital Audio

Name	Location	Dir	Type	Description
CLK_AU	H2	O	CMOS	Master clock for external audio codec
I2S_CLK	L2	I/O	CMOS	I2S Controller audio bit clock
I2S_SI	M4	I	CMOS	I2S Controller serial data in
I2S_SO	L3	O	CMOS	I2S Controller serial data out
I2S_WS	M5	I/O	CMOS	I2S Controller word select

Table 3-5. I2S Controller Pins.

3.2.5 Pins: Ethernet Interface

Name	Location	Dir	Type	Description
ENET_CRS_DV	P9	I/O	CMOS	Carrier sense
ENET_REF_CLK	T10	I/O	CMOS	Reference clock
ENET_RX_ER	T12	I/O	CMOS	Receive data error
ENET_RXD_0	R9	I/O	CMOS	Receive data
ENET_RXD_1	R10	I/O	CMOS	
ENET_TXD_0	T11	I/O	CMOS	Transmit data
ENET_TXD_1	M7	I/O	CMOS	
ENET_TXEN	M8	I/O	CMOS	Transmit ready

Table 3-6. Ethernet Pins.

3.2.6 Pins: USB

Name	Location	Dir	Type	Description
GPIO_2	F3	I/O	CMOS	USB EHCI over current detect input
GPIO_4	G2	I/O	CMOS	USB EHCI port power enable output
DETECT_VBUS	P6	I/O	CMOS	USB slave bus detect
USB0_DM	T1	I/O	Analog	USB0 data. DP/DM are differential signals.
USB0_DP	R1	I/O	Analog	
USB0_REXT	P1	I/O	Analog	USB0 resistor

Table 3-7. USB Interface Pins.

3.2.7 Pins: Smart Media Input/Output (SMIO)

- The Smart Media Input/Output (SMIO) pins are CMOS type and programmable input/output.
- SMIO pins are shared by controllers for NAND Flash (NAND) and SD.
- SMIO pins use **SMIO_[N]** for the primary function name.

Name	GPIO	Loc.	NAND		SD		Description
			Function	Dir	Function	Dir	
SMIO_0	55	M13	nand_ce	O			NAND chip enable
SMIO_1	56	N16	nand_rb	I/O			NAND ready / busy
SMIO_2	57	J13			sd_clk	O	SD0 clock
SMIO_3	58	K16			sd_cmd	I/O	SD0 command
SMIO_4	59	M12			sd_cd	I/O	SD0 card detect
SMIO_5	60	L12			sd_wp	I/O	SD0 write protect
SMIO_6	61	M14	nand_re	O			NAND read enable
SMIO_7	62	N15	nand_we	O			NAND write enable
SMIO_8	63	M15	nand_ale	O			NAND address latch enable
SMIO_9	64	L15	nand_d[0]	I/O			NAND data
SMIO_10	65	L13	nand_d[1]	I/O			NAND data
SMIO_11	66	L14	nand_d[2]	I/O			NAND data
SMIO_12	67	P16	nand_d[3]	I/O			NAND data
SMIO_13	68	R16	nand_d[4]	I/O			NAND data
SMIO_14	69	R15	nand_d[5]	I/O			NAND data
SMIO_15	70	P15	nand_d[6]	I/O			NAND data
SMIO_16	71	M16	nand_d[7]	I/O			NAND data
SMIO_17	72	N14	nand_cle	O			NAND command latch enable
SMIO_18	73	L16			sd_d[0]	I/O	SD0 data
SMIO_19	74	K15			sd_d[1]	I/O	SD0 data
SMIO_20	75	H13			sd_d[2]	I/O	SD0 data
SMIO_21	76	K10			sd_d[3]	I/O	SD0 data
WP	54	P4	nand_wp			I/O	NAND write protect

Table 3-8. Storage Media Interface Pins (SMIO) in NAND Flash and SD Modes.

3.2.8 Pins: SSI / SPI

Name	Location	Dir	Pad Type	Description
SSI0CLK	M3	I/O	CMOS	ssi0 master port bit clock
SSI0EN0	M2	O	CMOS	ssi0_en0 device enable
SSI0EN1	L1	O	CMOS	ssi0_en1 device enable
TIMER2	L4	I/O	CMOS	ssi0_en3 device enable
ENET_RXD_0	R9	I/O	CMOS	ssi1_en0 device enable
ENET_RXD_1	R10	I/O	CMOS	ssi1_en1 device enable
ENET_RX_ER	T12	I/O	CMOS	ssi1_en2 device enable

Name	Location	Dir	Pad Type	Description
ENET_CRS_DV	P9	I/O	CMOS	ssi1_en3 device enable
SSI0MISO	M1	I	CMOS	ssi0 master port data in
SSI0MOSI	N1	O	CMOS	ssi0 master port data out

Table 3-9. SSI / SPI Interface Pins.

3.2.9 Pins: IDC

Name	Location	Dir	Pad Type	Description
IDCCLK	R6	I/O	CMOS	First IDC serial port - clock
IDCDATA	N2	I/O	CMOS	First IDC serial port - data
IDC3CLK	N3	I/O	CMOS	Third IDC serial port - clock
IDC3DATA	N4	I/O	CMOS	Third IDC serial port - data

Table 3-10. IDC Interface Pins.

3.2.10 Pins: UART

Name	Location	Dir	Pad Type	Description
UART0RX	N5	I	CMOS	UART Port 0 receive
UART0TX	P3	O	CMOS	UART Port 0 transmit

Table 3-11. UART Interface Pins.

3.2.11 Pins: InfraRed Remote

Name	Location	Dir	Pad Type	Description
IR_IN	N6	I	CMOS	InfraRed input

Table 3-12. InfraRed Remote Interface Pins.

3.2.12 Pins: General Purpose Input/Output (GPIO)

The table below lists the General-Purpose Input/Output (GPIO) pins on the S2L55m chip. GPIO pins have multi-function capabilities and are CMOS-type programmable input/output. The function name that appears on the chip ball map is indicated in the **Pin Name** column. For complete function selection information, refer to the "S2L *Hardware Programming Reference Manual*".

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
2	**GPIO_2**	ehci_app_prt_ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1	
4	**GPIO_4**	ehci_prt_pwr_1	uart_ahb_rts_n	ssis_en	sc_c3	
24	**TIMER0**	tm11_clk			enet_2nd_ref_clk	
25	**TIMER1**	tm12_clk		idsp_pip_iopad_master_hsync	enet_mdc	
26	**TIMER2**	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync	enet_mdio	
27	**IDCCLK**	idc0clk				
28	**IDCDATA**	idc0data				
31	**IDC3CLK**	idc2clk	vin_strig0			
32	**IDC3DATA**	idc2data	vin_strig1			
33	**IR_IN**	ir_in				
34	**SSI0CLK**	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk	
35	**SSI0MOSI**	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd	
36	**SSI0MISO**	ssi0_rxd	norspi_dq[1]	uart_ahb_cts_n	ssis_txd	
37	**SSI0EN0**	ssi0_en0	norspi_en[0]	uart_ahb_rts_n	ssis_en	
38	**SSI0EN1**	ssi0_en1	norspi_en[1]			
39	**UART0RX**	uart0rx	uart_ahb_rx			
40	**UART0TX**	uart0tx	uart_ahb_tx			
41	**I2S_CLK**	i2s_clk				
42	**I2S_SI**	i2s_si				
43	**I2S_SO**	i2s_so				
44	**I2S_WS**	i2s_ws				
45	**CLK_AU**					
46	**ENET_TXEN**	enet_txen	sc_a0	enet_txen	ssi1_sclk	norspi_clk
47	**ENET_TXD_0**	enet_txd_0	sc_a1	enet_txd_0	ssi1_txd	norspi_dq[0]
48	**ENET_TXD_1**	enet_txd_1	sc_a2	enet_txd_1	ssi1_rxd	norspi_dq[1]
49	**ENET_RXD_0**	enet_rxd_0	sc_a3	enet_rxd_0	ssi1_en0	norspi_en[0]
50	**ENET_RXD_1**	enet_rxd_1	sc_b0	enet_rxd_1	ssi1_en1	norspi_en[1]
51	**ENET_RX_ER**	enet_rxer	sc_b1	enet_rxer	ssi1_en2	norspi_en[2]
52	**ENET_CRS_DV**	enet_crs_dv	sc_b2	enet_crs_dv	ssi1_en3	norspi_dq[2]
53	**ENET_REF_CLK**	enet_ref_clk	sc_b3	enet_rx_clk		norspi_dq[3]
54	**WP**		nand_wp			

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
55	**SMIO_0**		nand_ce	norspi_clk		
56	**SMIO_1**		nand_rb	norspi_dq[4]		
57	**SMIO_2**		sd_clk			
58	**SMIO_3**		sd_cmd			
59	**SMIO_4**		sd_cd			
60	**SMIO_5**		sd_wp			
61	**SMIO_6**		nand_re	norspi_dq[5]		
62	**SMIO_7**		nand_we	norspi_dq[6]		
63	**SMIO_8**		nand_ale	norspi_dq[7]		
64	**SMIO_9**		nand_d[0]	norspi_en[0]		
65	**SMIO_10**		nand_d[1]	norspi_en[1]		
66	**SMIO_11**		nand_d[2]	norspi_en[2]		
67	**SMIO_12**		nand_d[3]	norspi_en[3]		
68	**SMIO_13**		nand_d[4]	norspi_dq[0]		
69	**SMIO_14**		nand_d[5]	norspi_dq[1]		
70	**SMIO_15**		nand_d[6]	norspi_dq[2]		
71	**SMIO_16**		nand_d[7]	norspi_dq[3]		
72	**SMIO_17**		nand_cle			
73	**SMIO_18**		sd_d[0]			
74	**SMIO_19**		sd_d[1]			
75	**SMIO_20**		sd_d[2]			
76	**SMIO_21**		sd_d[3]			
91	**SVSYNC**	vin_svsync	idsp_pip_iopad_master_hsync			
92	**SHSYNC**	vin_shsync	idsp_pip_iopad_master_vsync			
93	**VD0_OUT_0**	vd0_out[0]				
94	**VD0_OUT_1**	vd0_out[1]				
95	**VD0_OUT_2**	vd0_out[2]				
96	**VD0_OUT_3**	vd0_out[3]				
97	**VD0_OUT_4**	vd0_out[4]				
98	**VD0_OUT_5**	vd0_out[5]				
99	**VD0_OUT_6**	vd0_out[6]				
100	**VD0_OUT_7**	vd0_out[7]				
101	**VD0_OUT_8**	vd0_out[8]				
102	**VD0_OUT_9**	vd0_out[9]				
103	**VD0_OUT_10**	vd0_out[10]				
104	**VD0_OUT_11**	vd0_out[11]				
105	**VD0_OUT_12**	vd0_out[12]				
106	**VD0_OUT_13**	vd0_out[13]				
107	**VD0_OUT_14**	vd0_out[14]				
108	**VD0_OUT_15**	vd0_out[15]				

GPIO	Pin Name	Multiplexed Function				
		First	Second	Third	Fourth	Fifth
109	**VD0_CLK**	vd0_clk				
110	**VD0_VSYNC**	vd0_vsync				
111	**VD0_HSYNC**	vd0_hsync				
112	**VD0_HVLD**	vd0_hvld				
113	**VD_PWM**	pwm_0				

Table 3-13. General Purpose Input Output (GPIO) Multifunction-Capable Pins.

3.2.13 Pins: Analog to Digital Conversion (ADC)

Name	Location	Dir	Type	Description
ADC_CH_[1:2]	A4, A3	I	Analog	ADC analog input (2 channels)
ADC_VDD18	A6	S	Analog Supply	ADC digital power supply
ADC_VDDA33	A2	S	Analog Supply	ADC analog power supply

Table 3-14. ADC Interface Pins.

3.2.14 Pins: Power Controller (PWC) and Real Time Clock (RTC)

Name	Location	Dir	Type	Description
PWC_PC_REF	B1	I/O	Analog	Used to detect whether battery level is too low. Connect to voltage-divided version of **PWC_PC_VDD.**
PWC_PSEQ1	B6	O	CMOS	Power Up/Down control signals.
PWC_RSTINB	B4	I	CMOS	PWC reset input. Usually pulled up to **PWC_PC_VDD** through an RC circuit.
PWC_RTC_CP	C1	S	Analog Supply	Power for RTC module and on-chip RTC oscillator. When **PWC_RTC_CP** is less than a specified voltage, the power controller will shut down and all registers will reset.
PWC_WKUP	A1	I	CMOS	In the power-off state, a positive pulse can only trigger a power on sequence.
XI_RTC	B5	I	XOSC	Connect to RTC crystal
XO_RTC	A5	O	XOSC	Connect to RTC crystal
PWC_PC_VDD	B2	S	Digital Supply	Power for power-management module Connected to external battery/adaptor clamping circuit. The **PWC_PC_VDD** voltage must be a specified minimum to block a **WKUP[N]**.

Table 3-15. PWC and RTC Interface Pins.

3.2.15 Pins: Timer

Name	Location	Dir	Type	Description
TIMER0	K4	I/O	CMOS	Interval Timer 0 external clock source
TIMER1	K3	I/O	CMOS	Interval Timer 1 external clock source
TIMER2	L4	I/O	CMOS	Interval Timer 2 external clock source

Table 3-16. Timer Pins.

3.2.16 Pins: Pulse Width Modulator (PWM)

Name	Location	Dir	Type	Description
VD_PWM	M10	I/O	CMOS	Pulse Width Modulator Output

Table 3-17. PWM Pins.

3.2.17 Pins: JTAG Control

Name	Location	Dir	Pad Type	Description
JTAG_CLK	B3	I	CMOS	Clock
JTAG_RST_L	C3	I	CMOS	Reset
JTAG_TDI	E2	I	CMOS	Data in
JTAG_TDO	D3	O	CMOS	Data out
JTAG_TMS	C2	I	CMOS	Test mode select

Table 3-18. JTAG Pins.

3.2.18 Pins: Global and Test

Name	Location	Dir	Type	Description
FSOURCE_0	J16	S	Power / Ground	Power supply during programming. Customer ties to digital ground for operation.
POR_L	M6	I	CMOS	Power-on reset pin (active low)
TEST_MODE	L11	I	CMOS	0 - Normal mode 1 - Test mode
XIN	K1	I	XOSC	24-MHz or 48-MHz crystal or crystal oscillator input
XOUT	J2	O	XOSC	

Table 3-19. Global and Test Pins.

3.2.19 Pins: Power, Ground and PLL

Name	Location	Dir	Type	Description
ADC_VDD18	A6	S	Analog Supply	ADC digital power supply
ADC_VDDA33	A2	S	Analog Supply	ADC analog power supply
DDR_VDDQ_[L]	C4, C5, C6, C7, C8, C9, C10, D11	S	Digital Supply	DDR digital I/O power supply
MIPI_VDDIO	T9	S	Analog Supply	VIN digital power
PWC_PC_VDD	B2	S	Digital Supply	Power for power management module Connected to external battery/adaptor clamping circuit. The **PWC_PC_VDD** voltage must be a specified minimum to block a **WKUP[N]**.
VDD_[L]	F4, F12, G3 G4, G12, H3, H4, H12, J3, J4, J5, J6, J7, J12, K11, K12	S	Digital Supply	Digital power supply
VDD18_[L]	L5, L6, L7, L8	S	Digital Supply	Digital power supply
VDD33_[L]	K5, K6, K7, K8, K9	S	Digital Supply	Digital power supply
NAND_VDDO_[L]	K13, K14	S	Digital Supply	NAND Flash digital power
VDDA	G1, H1	S	Analog Supply	Analog power supply
VDDA33	D2, T2	S	Analog Supply	Analog power supply
VSS_[L]	D4, D5, D6, D7, D8, D9, D10, E3, E4, E5, E6, E7, E8, E9, E10, E11, F5, F6, F7, F8, F9, F10, F11, G5 G6, G7, G8, G9, G10, G11, H5, H6, H7, H8, H9, H10, H11, J10, J11	G	Digital Ground	Digital ground

Table 3-20. Power, Ground and PLL Pins.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical: Overview

This section provides details on the electrical characteristics of the S2L55m chip as follows:

- (Section 4.1) Electrical: Overview
- (Section 4.2) Electrical: Absolute Ratings
- (Section 4.3) Electrical: Recommended Operating Conditions
- (Section 4.4) Electrical: Fail-Safe Pins
- (Section 4.5) Electrical: Video Signal Wave Forms and Timing
- (Section 4.6) Electrical: SD Controller Timing

Note that the electrical details provided in this section are preliminary estimates.

4.2 Electrical: Absolute Ratings

The following table provides absolute ratings for the nominal analog / digital voltages of the S2L55m power rails.

Parameter	Minimum	Maximum
Analog supply voltage (3.0 V)	-0.3 V	3.6 V
Digital supply voltage (3.0 V)	-0.3 V	3.6 V
Analog supply voltage (1.8 V)	-0.3 V	1.98 V
Digital supply voltage (1.8 V)	-0.3 V	1.98 V
Analog supply voltage (1.1 V)	-0.3 V	1.15 V
Digital supply voltage (1.1 V)	-0.3 V	1.15 V
Digital I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Analog I/O range (V)	-0.3 V	3.6 V
	-0.3 V	1.98 V
Operating temperature (case) (°C)	0 C to 70 C	
Storage temperature (°C)	-40 C to +85 C	
Thermal resistance (Θ_{jc}) (°C/W)	TBD	

Table 4-1. Absolute Ratings.

This Ambarella part will support a full range of operation at the case temperature specified above, provided that the customer's PCB design, manufacturing processes, and power supply design are equal to those of the Ambarella reference hardware platform in terms of quality. All other components used during system design are also required to operate successfully at the case temperature range specified above to guarantee proper overall system operation.

4.3 Electrical: Recommended Operating Conditions

This section continues with recommended operating conditions for:

- (Section 4.3.1) Operating Conditions: Power Rails - DC Characteristics
- (Section 4.3.2) Operating Conditions: Digital I/O
- (Section 4.3.3) Operating Conditions: DRAM I/O
- (Section 4.3.4) Operating Conditions: PWC and RTC Power Supply
- (Section 4.3.5) Operating Conditions: Video Sensor Input
- (Section 4.3.6) Operating Conditions: Video DAC
- (Section 4.3.7) Operating Conditions: ADC Electrical Specifications
- (Section 4.3.8) Operating Conditions: Crystal and Reference Clock Requirements

4.3.1 Operating Conditions: Power Rails - DC Characteristics

Parameter [1]	Comments	Minimum	Typical	Maximum	Ripple
ADC_VDD18	Channel 0	1.7 V	1.8 V	1.9 V	2%
ADC_VDDA33	All other channels	2.85 V	3.0 V	3.15 V	2%
DDR_VDDQ_CKE / DDR_VDDQ	DDR3 Mode	1.4 V	1.5 V	1.6 V	2%
	DDR3L Mode	1.28 V	1.35 V	1.45 V	2%
MIPI_VDDIO	Sensor SLVS/MIPI Mode	1.04 V	1.1 V	1.15 V	2%
	Sensor 1.8-V LVCMOS	1.7 V	1.8 V	1.9 V	2%
PWC_PC_VDD		2.9 V	3.1 V	3.15 V	2%
VDAC_AVDD18		1.7 V	1.8 V	1.9 V	2%
VDAC_AVDD33		2.85 V	3.0 V	3.15 V	2%
VDD		1.04 V	1.1 V	1.15 V	2%
VDD33		2.85 V	3.0 V	3.15 V	2%
NAND_VDDO	3.0-V mode	2.85 V	3.0 V	3.15 V	2%
	1.8-V mode	1.7 V	1.8 V	1.9 V	2%
VDD18		1.7 V	1.8 V	1.9 V	2%

Table 4-2. Power Rails: DC Characteristics (Preliminary and Subject to Change).

Note:

1. The electrical details provided in this section are preliminary estimates and are subject to change. Please contact an Ambarella representative for current electrical specifications.

4.3.2 Operating Conditions: Digital I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	Input Low Voltage	-0.3 V		0.7 V
VIH	Input High Voltage	2.0 V		3.6 V (for 3.3 V-tolerant pins)
VOL	Output Low Voltage			0.4 V
VOH	Output High Voltage	2.4 V		

Table 4-3. Digital I/O Characteristics (Preliminary).

4.3.3 Operating Conditions: DRAM I/O

4.3.3.1 DRAM: DC Supply Voltage Levels

Parameter	Comments	Minimum	Typical	Maximum
DDR_VDDQ		See Section 4.3.1		
DDR_VDDQ_CKE		See Section 4.3.1		
VTT	Termination voltage	DDR_VREF - 0.04 V	DDR_VREF	DDR_VREF + 0.04 V
DDR_VREF	Input reference level	0.49 * DDR_VDDQ	0.5 * VDDQ	0.51 * DDR_VDDQ

Table 4-4. DRAM I/O Characteristics - DC Supply Voltage Levels (Preliminary).

4.3.3.2 DRAM: SSTL18 I/O DC Specifications

Parameter	Comments	Minimum	Typical	Maximum
VIHT	DC input logic threshold high			DDR_VREF + 0.05 V
VILT	DC input logic threshold low	DDR_VREF - 0.05 V		
VIH	DC input voltage high	TBD		VDDQ + 0.3 V
VIL	DC input voltage low	-0.3 V		
VOH	DC output logic high	DDR_VDDQ		
VOL	DC output logic low			0 V
RTT1	RTT effective impedance	60 Ohms	75 Ohms	90 Ohms
RTT2	RTT effective impedance	120 Ohms	150 Ohms	180 Ohms

Table 4-5. DRAM I/O Characteristics - SSTL18 I/O DC Specifications (Preliminary).

4.3.4 Operating Conditions: PWC and RTC Power Supply

Parameter	Comments	Minimum	Typical	Maximum
PWC_RTC_CP	RTC module supply	1.2 V	2.4 V	2.6 V
PWC_PC_VDD	Power management supply	2.9 V	3.1 V	3.15 V
PWC_PC_REF	Reference voltage	1.3 V		1.8 V
VIH	For PWC_WKUP	0.7 * PWC_RTC_CP		
VIL	For PWC_WKUP			0.3 * PWC_RTC_CP
VOH	PWC_PSEQ[1:3]	0.9 * PWC_PC_VDD		
	PWC_RSTOB	TBD	TBD	TBD

Table 4-6. PWC and RTC Supply.

4.3.5 Operating Conditions: Video Sensor Input

4.3.5.1 VIN: SLVS / LVCMOS I/O

Parameter	Comments	Minimum	Typical	Maximum
VIL	MIPI_VDDA11			0.45 V
	MIPI_VDDA18			0.6 V
VIH	MIPI_VDDA11	1.35 V		
	MIPI_VDDA18	1.62 V		

Table 4-7. SLVS / LVCMOS I/O.

4.3.5.2 VIN: MIPI Receiver DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VIH	Logic 1 input voltage	880 mV		
VIL	Logic 0 input voltage, not in ULP state			550 mV
VIL-ULP	Logic 0 input voltage, ULP state			300 mV
VHYST	Input hysteresis	25 mV		

Table 4-8. MIPI Receiver DC Specification.

4.3.5.3 VIN: MIPI Receiver AC Specification

Description	Minimum	Typical	Maximum
Input pulse rejection			300 V-ps
Minimum pulse width response	20 ns		
Peak interference amplitude			200 mV
Interference frequency	450 MHz		

Table 4-9. MIPI Receiver AC Specification.

4.3.6 Operating Conditions: Video DAC

Parameter	Comments	Minimum	Typical	Maximum
VDD	Operating digital supply voltage	1.04 V	1.1 V	1.15 V
IO_{FS}	IO out current		34.6 mA	
I_{OP}	Operating Current		36 mA	
V(IO)	Out voltage full scale	1.17 V	1.28 V	1.43 V
Resolution	DAC resolution			10 bits
DNL	Differential non-linearity error			±1 LSB
INL	Integral non-linearity error			±2 LSB
VREF	Reference Voltage			1.22 V

Table 4-10. Video DAC Electrical Specifications.

4.3.7 Operating Conditions: ADC Electrical Specifications

4.3.7.1 ADC Electrical: DC Specification

Parameter	Comments	Minimum	Typical	Maximum
VDD	Digital supply voltage	1.04 V	1.1 V	1.15 V
ADC_AVDD18	Analog supply (channel 0)	1.7 V	1.8 V	1.9 V
ADC_AVDD33	Analog supply (other channels)	2.85 V	3.0 V	3.15 V
IVDDA	Operating current (Fclk = 5 MHz and Fs = 1 MS/s)		4 mA	
VREF	Reference Voltage (Top) (Low reference is ADC_AVSS)	TBD	ADC_AVDD	ADC_AVDD
VIN	Analog input voltage	ADC_AVSS		VREF
N	Resolution		12 bits	
INL	INL		±1 LSB	±4 LSB
DNL	DNL		±0.5 LSB	±1 LSB
CIN	Input impedance	TBD	TBD	TBD

Table 4-11. ADC DC Specification.

4.3.7.2 ADC Electrical: AC Specification

Parameter	Comments	Minimum	Typical	Maximum
ENOB	Effective resolution		500 KS/s	1000 KS/s
Fs	Sampling rate			12 MHz
FCLK	Sampling clock		5 MHz	
SNDR	Signal-to-noise and distortion ratio (Fclk = 5 MHz and AIN = 50 KHz*)	54 dB	58 dB	TBD

Table 4-12. ADC AC Specification.

4.3.8 Operating Conditions: Crystal and Reference Clock Requirements

4.3.8.1 Crystal and Reference Clock Requirements: 24 or 48 MHz

Description	Minimum	Typical	Maximum
Crystal frequency	N/A	24 or 48 MHz only	N/A
Crystal accuracy			± 30 PPM
Cycle-to-cycle jitter			± 200 ps
Long-term jitter			± 500 ps

Table 4-13. Jitter Specifications (24 or 48 MHz).

4.3.8.2 Crystal and Reference Clock Requirements: 32.768 KHz

Description	Minimum	Typical	Maximum
Crystal accuracy			± 30 PPM

Table 4-14. Jitter Specifications (32.768 KHz).

4.4 Electrical: Fail-Safe Pins

The S2L55m chip provides a number of fail-safe CMOS pins that can have active signals at or below 3.6 V when the S2L55m is powered down. For fail-safe pin locations, please refer to Chapter 7.

Pin Name	Multiplexed Function					
	First	Second	Third	Fourth	Fifth	GPIO
GPIO_2	ehci_app_prt_ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1		2
GPIO_4	ehci_prt_pwr_1	uart_ahb_rts_n	ssis_en	sc_c3		4
TIMER0	tm11_clk			enet_2nd_ref_clk		24
TIMER1	tm12_clk		idsp_pip_iopad_master_hsync	enet_mdc		25
TIMER2	tm13_clk	ssi0_en3	idsp_pip_iopad_master_vsync	enet_mdio		26
IDCCLK	idc0clk					27
IDCDATA	idc0data					28
IDC3CLK	idc2clk	vin_strig0				31
IDC3DATA	idc2data	vin_strig1				32
IR_IN	ir_in					33
SSI0CLK	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk		34
SSI0MOSI	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd		35
SSI0MISO	ssi0_rxd	norspi_dq[1]	uart_ahb_cts_n	ssis_txd		36
SSI0EN0	ssi0_en0	norspi_en[0]	uart_ahb_rts_n	ssis_en		37
SSI0EN1	ssi0_en1	norspi_en[1]				38

Pin Name	Multiplexed Function					
	First	Second	Third	Fourth	Fifth	GPIO
UART0RX	uart0rx	uart_ahb_rx				39
UART0TX	uart0tx	uart_ahb_tx				40
I2S_CLK	i2s_clk					41
I2S_SI	i2s_si					42
I2S_SO	i2s_so					43
I2S_WS	i2s_ws					44
CLK_AU						45
WP		nand_wp				54
SMIO_0		nand_ce	norspi_clk			55
SMIO_2		sd_clk				57
SMIO_3		sd_cmd				58
SMIO_4		sd_cd				59
SMIO_5		sd_wp				60
SMIO_18		sd_d[0]				73
SMIO_19		sd_d[1]				74
SMIO_20		sd_d[2]				75
SMIO_21		sd_d[3]				76
SVSYNC	vin_svsync	idsp_pip_iopad_master_hsync				91
SHSYNC	vin_shsync	idsp_pip_iopad_master_vsync				92
VD0_CLK	vd0_clk					109
VD_PWM	pwm_0					113
DETECT_VBUS						
JTAG_TDO						

Table 4-15. Fail-Safe Pins Which Can Have Active Signals At or Below 3.6 V When the S2L55m is Powered Down.

4.5 Electrical: Video Signal Wave Forms and Timing

4.5.1 Video Waveform: Video Input (VIN) LVCMOS Timing

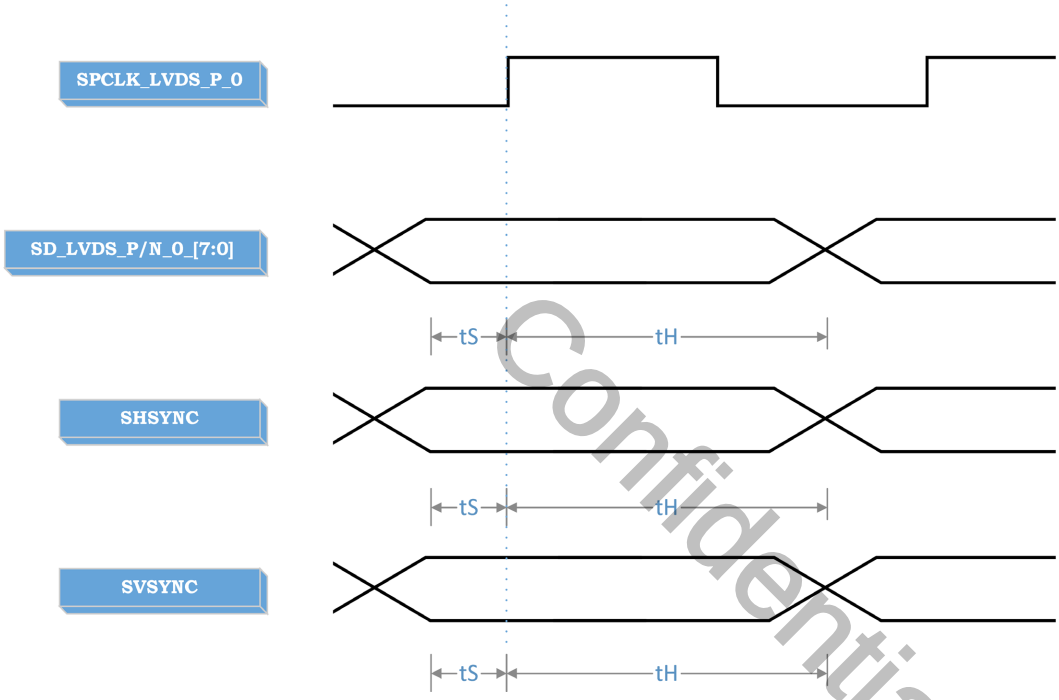


Figure 4-1. Video Input (VIN) LVCMOS Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_0_[7:0]**	2 ns	2 ns	Assume the rising edge of the pixel clock **SPCLK_LVDS_P_0** is used to latch the data.
HSync: **SHSYNC**	2 ns	2 ns	
VSync: **SVSYNC**	2 ns	2 ns	
SField:	2 ns	2 ns	

*Table 4-16. LVCMOS Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.2 Video Waveform: Video Input (VIN) SLVS/MIPI Timing

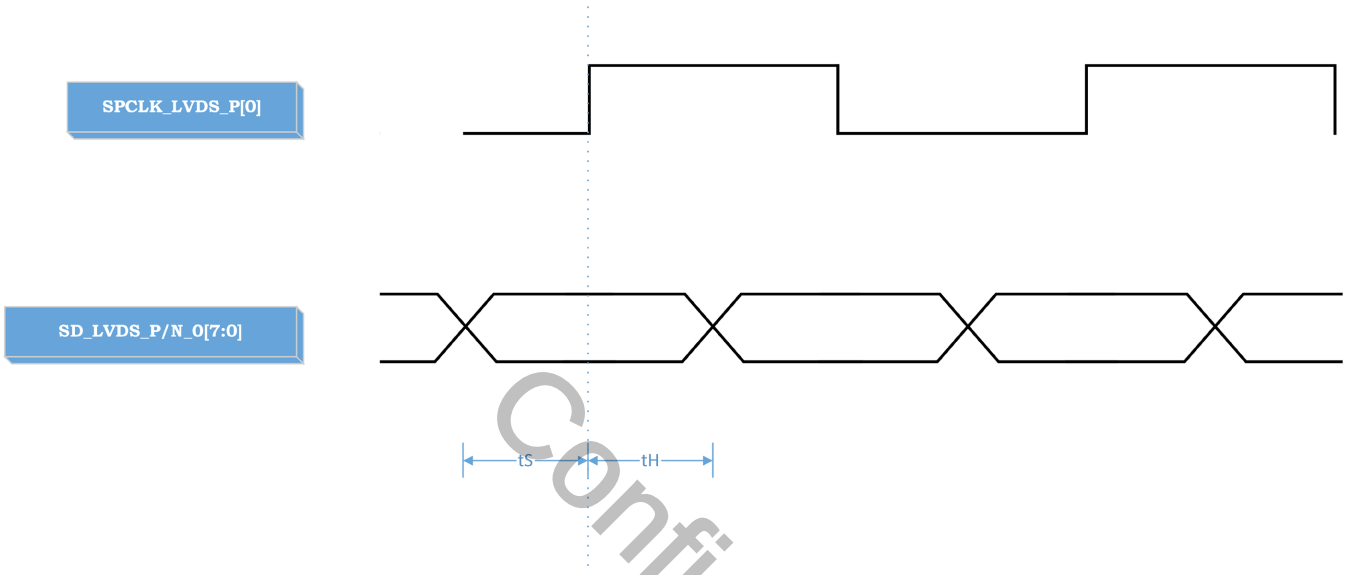


Figure 4-2. Video Input (VIN) SLVS/MIPI Timing.

Parameter	Setup (tS)	Hold (tH)	Comment
Data: **SD_LVDS_P/N_0_[7:0]**	150 ps	150 ps	Assume the rising edge of the pixel clock **SPCLK_LVDS_P[0]** is used to latch the data.

*Table 4-17. SLVS/MIPI Video Input Timing Setup/Hold With Respect to **SPCLK_LVDS_P/N_[N]**.*

4.5.3 Video Waveform: Video Output (VOUT) Timing

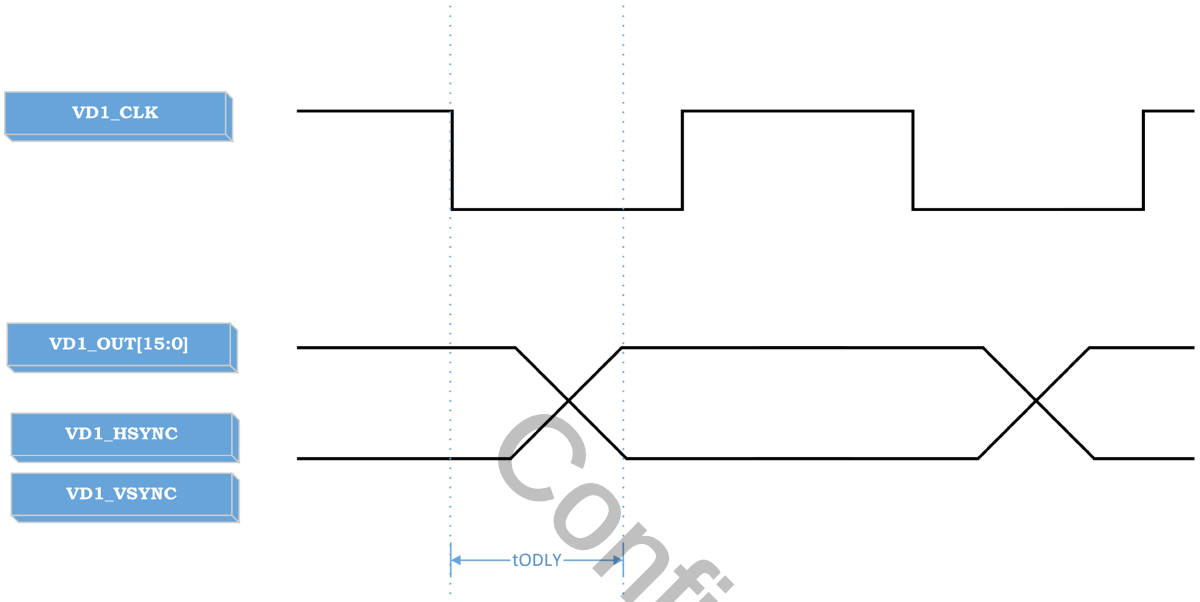


Figure 4-3. Video Output Timing.

Parameter	Minimum	Typical	Maximum	Comment
VD1_CLK Frequency		Resolution Dependent		Assume the data is latched out at the falling edge of **VD1_CLK**.
VD1_CLK Duty	40%	50%	60%	
tODLY Output Delay	-2 ns		2 ns	

*Table 4-18. Video Output Timing Setup/Hold With Respect to **VD1_CLK**.*

4.6 Electrical: SD Controller Timing

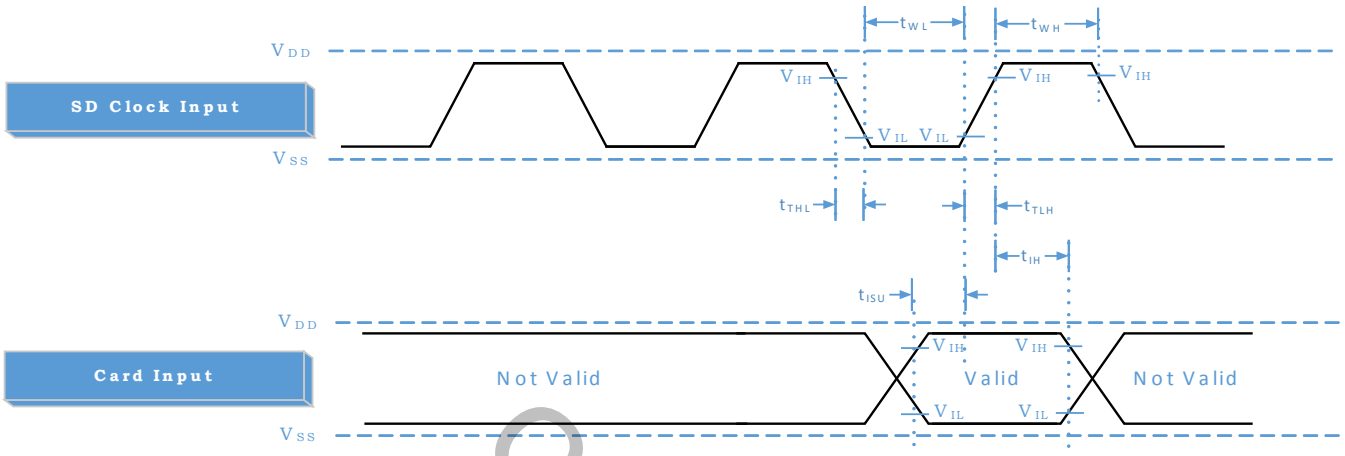


Figure 4-4. SD Card Input Timing.

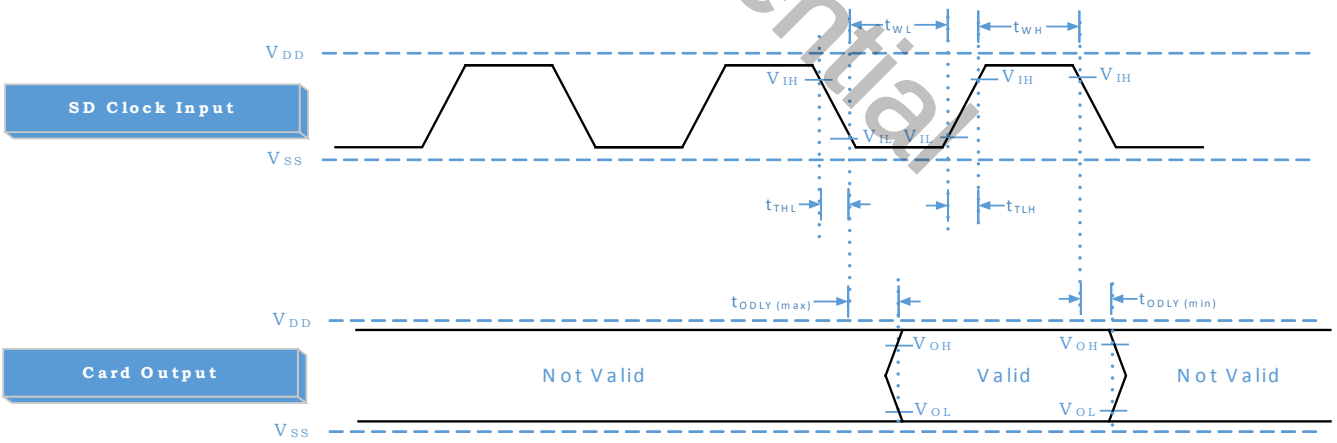


Figure 4-5. SD Card Output Timing.

Parameter	Symbol	Min	Max	Unit	Comment
Clock CLK: All values are referred to as min (VIH) and max (VIL)					
Clock Frequency: Data Transfer Mode	f_{PP}	0	25	MHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Frequency: Identification Mode	f_{OD}	0/100	400	kHz	C_{CARD} ≤ 10 pF (1 Card)
Clock Low Time	t_{WL}	10		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock High Time	t_{WH}	10		ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Rise Time	t_{TLH}		10	ns	C_{CARD} ≤ 10 pF (1 Card)
Clock Fall Time	t_{THL}		10	ns	C_{CARD} ≤ 10 pF (1 Card)
Inputs CMD, DAT: Referenced to CLK					
Input Set-Up Time	t_{ISU}	5		ns	C_{CARD} ≤ 10 pF (1 Card)
Input Hold Time	t_{IH}	5		ns	C_{CARD} ≤ 10 pF (1 Card)
Outputs CMD, DAT: Referenced to CLK					
Output Delay Time During Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 Card)
Output Delay Time During ID Mode	t_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 Card)

Table 4-19. SD Card Timing Parameters.

5. PACKAGE

The S2L55m chip has a 256-pin PBGA package (11 mm x 11 mm).

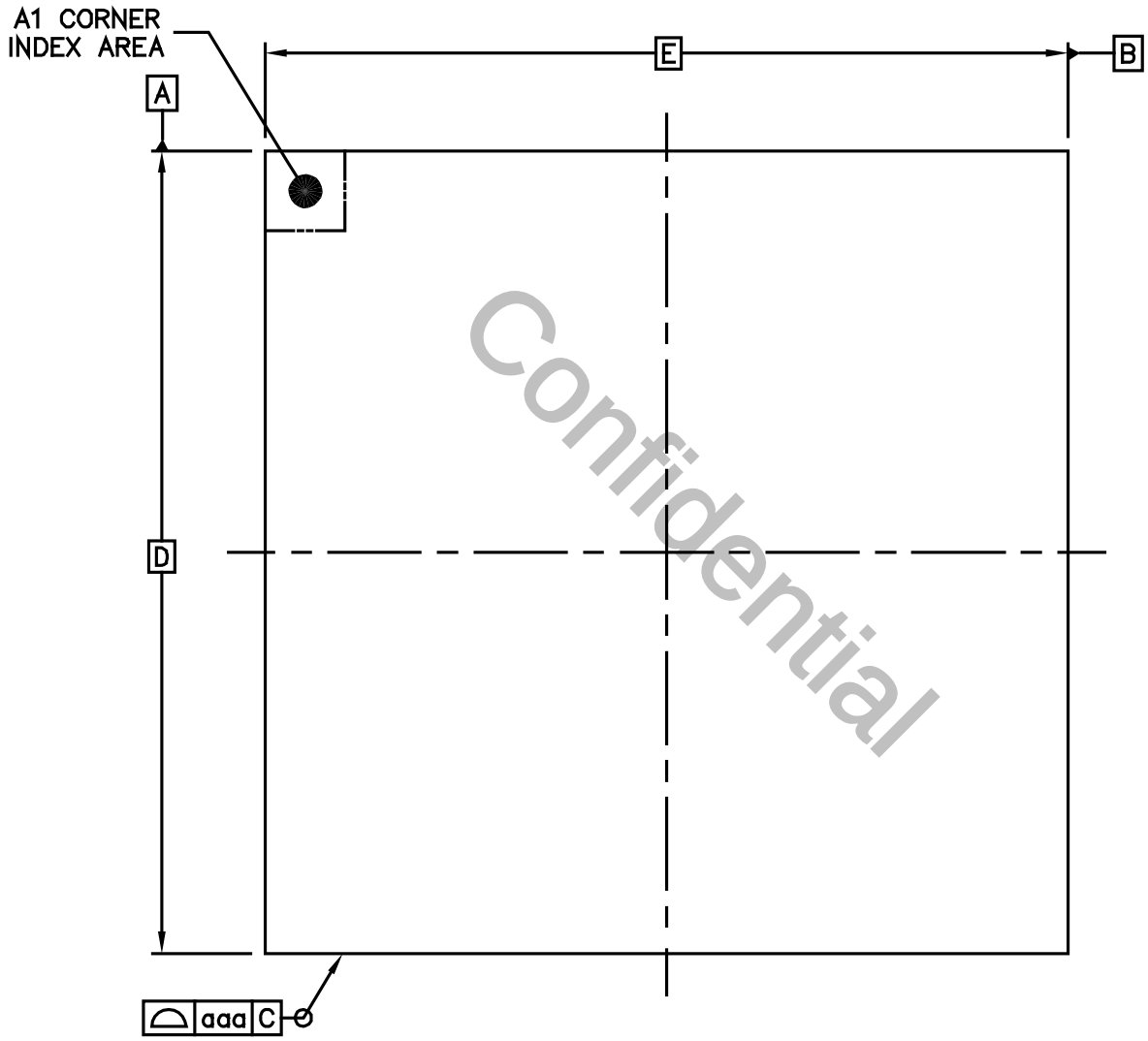


Figure 5-1. Top View of the S2L55m Package.

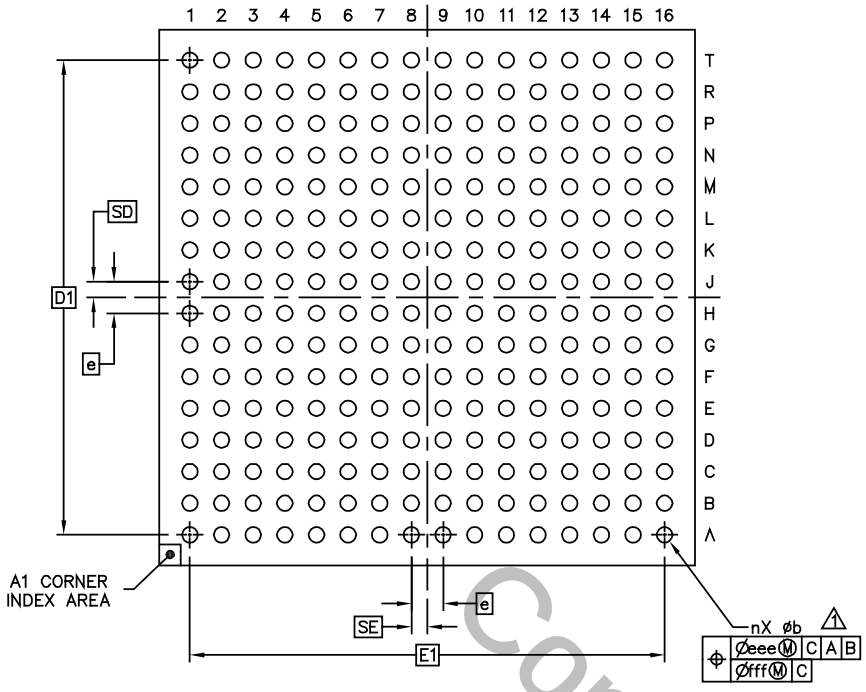


Figure 5-2. Bottom View of the S2L55m Package.

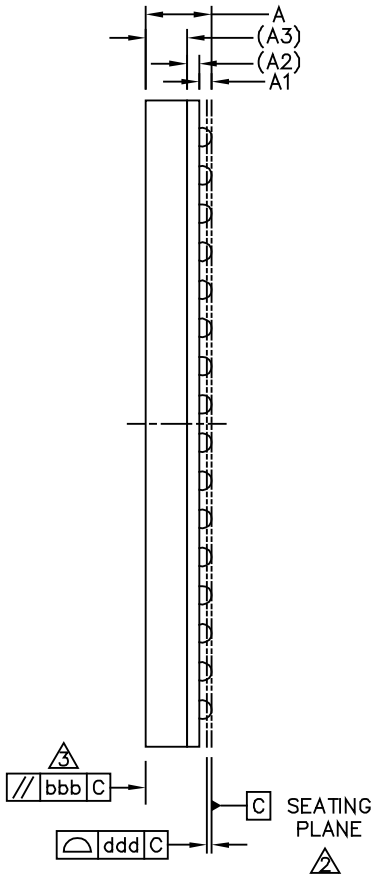


Figure 5-3. Side View of the S2L55m Package.

Description	Symbol	Minimum	Nominal	Maximum
Total Thickness	A			1.2
Stand Off	A1	0.16		0.26
Substrate Thickness	A2		0.21 REF	
Mold Thickness	A3		0.7 REF	
Body Size	D		11 BSC	
	E		11 BSC	
Ball Diameter			0.3	
Ball Opening			0.275	
Ball Width	b	0.27		0.37
Ball Pitch	e		0.65 BSC	
Ball Count	n		256	
Edge Ball Center to Center	D1		9.75 BSC	
	E1		9.75 BSC	
Body Center to Contact Ball	SD		0.325 BSC	
	SE		0.325 BSC	
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

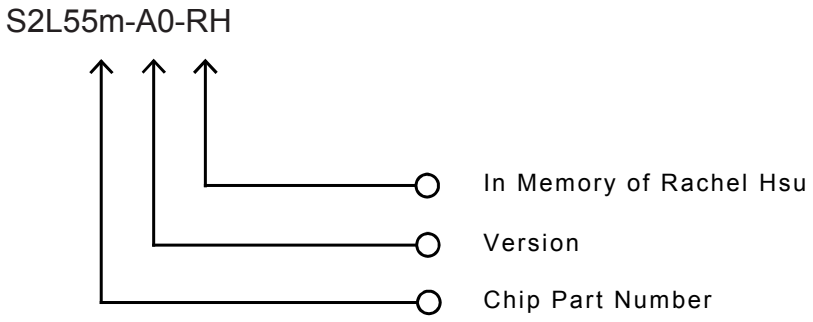
Table 5-1. Dimensions of the S2L55m Package (millimeters).

Notes for table and figures:

1. All dimensions are in millimeters.
2. Dimension b is measured at the maximum solder ball diameter, parallel to Datum Plane C.
3. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
4. Parallelism measurement excludes any effect of mark on top surface of the package.
5. Dimension and Tolerances: ASME Y14.5M

6. CONTACT AND ORDER INFORMATION

All chips in the S2L series are Lead-Free, Halogen-Free and RoHS compliant.



US
3101 Jay St.
Ste. 110
Santa Clara, CA 95054, USA
Phone: +1.408.734.8888
Fax: +1.408.734.0788

Taiwan
Suite C1, No. 1, Li-Hsin Road 1
Science-Based Industrial Park
Hsinchu 30078, Taiwan
Phone: +886.3.666.8828
Fax: +886.3.666.1282

Korea
6 Floor, Hanwon-Bldg.
Sunae-Dong, 6-1, Bundang-Gu
SeongNam-City, Kyunggi-Do
Republic of Korea 463-825
Phone: +031.717.2780
Fax: +031.717.2782

Japan - Yokohama
Shin-Yokohama Business Center Bldg. 5th Floor
3-2-6 Shin-Yokohama, Kohoku-ku,
Yokohama, Kanagawa, 222-0033, Japan
Phone: +81.45.548.6150
Fax: +81.45.548.6151

Hong Kong
Unit A&B, 18/F, Spectrum Tower
53 Hung To Road
Kwun Tong, Kowloon
Phone: +85.2.2806.8711
Fax: +85.2.2806.8722

China - Shenzhen
Unit E, 5th Floor
No. 2 Finance Base
8 Ke Fa Road
Shenzhen, 518057, China
Phone: +86.755.3301.0366
Fax: +86.755.3301.0966

China - Shanghai
9th Floor, Park Center
1088 Fangdian Road, Pudong New District
Shanghai 201204, China
Phone: +86.21.6088.0608
Fax: +86.21.6088.0366

7. PIN LIST AND MAPPING TABLE

This section provides a list of the 256 external pins according to their location on the S2L55m chip. Figure 7-1 below indicates the orientation of the pins by column (numbers) and row (letters).

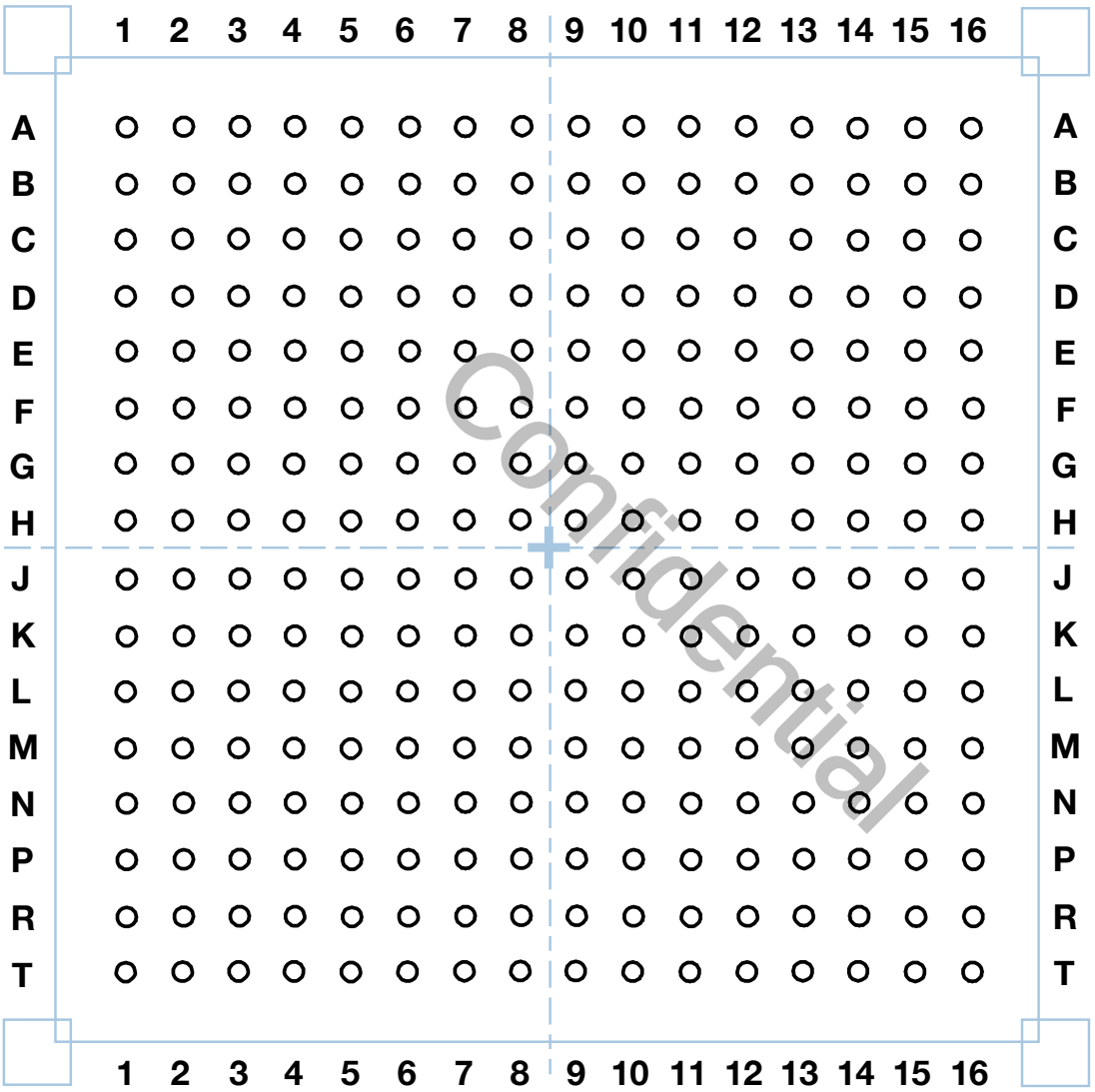


Figure 7-1. Pin Map for the S2L55m Chip.

The table below lists all of the external pins on the S2L55m chip in alphabetic order by map location. Each entry provides the pin name as it appears on the ball map, the location of the pin on the map and on schematics, the functional group, and multiplexed functionality detail if applicable.

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A1	**PWC_WKUP**	PWC	Analog						
A2	**ADC_VDDA33**	Power	Analog Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
A3	**ADC_CH_2**	ADC	Analog						
A4	**ADC_CH_1**	ADC	Analog						
A5	**XO_RTC**	Global	Analog						
A6	**ADC_VDD18**	Power	Digital Supply						
A7	**DDR_DM_1**	DDR	SSTL						
A8	**DDR_DQS_1**	DDR	SSTL						
A9	**DDR_DQ_14**	DDR	SSTL						
A10	**DDR_DQ_12**	DDR	SSTL						
A11	**DDR_DQ_10**	DDR	SSTL						
A12	**DDR_DQS_BAR_0**	DDR	SSTL						
A13	**DDR_DQ_5**	DDR	SSTL						
A14	**DDR_DQ_3**	DDR	SSTL						
A15	**DDR_DQ_0**	DDR	SSTL						
A16	**DDR_CK**	DDR	SSTL						
B1	**PWC_PC_REF**	PWC	Analog						
B2	**PWC_PC_VDD**	PWC	Digital Supply						
B3	**JTAG_CLK**	JTAG	CMOS						
B4	**PWC_RSTINB**	PWC	Analog						
B5	**XI_RTC**	Global	Analog						
B6	**PWC_PSEQ1**	PWC	Analog						
B7	**DDR_CALIBR**	DDR	SSTL						
B8	**DDR_DQS_BAR_1**	DDR	SSTL						
B9	**DDR_DQ_15**	DDR	SSTL						
B10	**DDR_DQ_13**	DDR	SSTL						
B11	**DDR_DQ_11**	DDR	SSTL						
B12	**DDR_DQS_0**	DDR	SSTL						
B13	**DDR_DQ_4**	DDR	SSTL						
B14	**DDR_DQ_2**	DDR	SSTL						
B15	**DDR_DQ_1**	DDR	SSTL						
B16	**DDR_CK_BAR**	DDR	SSTL						
C1	**PWC_RTC_CP**	PWC	CMOS						
C2	**JTAG_TMS**	JTAG	CMOS						
C3	**JTAG_RST_L**	JTAG	CMOS						
C4	**DDR_VDDQ_C4**	Power	DDR HOST Supply						
C5	**DDR_VDDQ_C5**	Power	DDR HOST Supply						
C6	**DDR_VDDQ_C6**	Power	DDR HOST Supply						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
C7	**DDR_VDDQ_C7**	Power	DDR HOST Supply						
C8	**DDR_VDDQ_C8**	Power	DDR HOST Supply						
C9	**DDR_VDDQ_C9**	Power	DDR HOST Supply						
C10	**DDR_VDDQ_C10**	Power	DDR HOST Supply						
C11	**DDR_VREF**	Power	DDR HOST Supply						
C12	**DDR_DQ_9**	DDR	SSTL						
C13	**DDR_DQ_7**	DDR	SSTL						
C14	**DDR_DQ_6**	DDR	SSTL						
C15	**DDR_ADDR_4**	DDR	SSTL						
C16	**DDR_ADDR_8**	DDR	SSTL						
D1	**DAC_IO**	DAC	Analog						
D2	**VDDA33_D2**	Power	Analog Supply						
D3	**JTAG_TDO**	JTAG	CMOS						
D4	**VSS_D4**	Power	Ground						
D5	**VSS_D5**	Power	Ground						
D6	**VSS_D6**	Power	Ground						
D7	**VSS_D7**	Power	Ground						
D8	**VSS_D8**	Power	Ground						
D9	**VSS_D9**	Power	Ground						
D10	**VSS_D10**	Power	Ground						
D11	**DDR_VDDQ_D11**	Power	DDR HOST Supply						
D12	**DDR_DQ_8**	DDR	SSTL						
D13	**DDR_DM_0**	DDR	SSTL						
D14	**DDR_ADDR_7**	DDR	SSTL						
D15	**DDR_ADDR_6**	DDR	SSTL						
D16	**DDR_ADDR_9**	DDR	SSTL						
E1	**DAC_VREFIN**	DAC	Analog						
E2	**JTAG_TDI**	JTAG	CMOS						
E3	**VSS_E3**	Power	Ground						
E4	**VSS_E4**	Power	Ground						
E5	**VSS_E5**	Power	Ground						
E6	**VSS_E6**	Power	Ground						
E7	**VSS_E7**	Power	Ground						
E8	**VSS_E8**	Power	Ground						
E9	**VSS_E9**	Power	Ground						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
E10	**VSS_E10**	Power	Ground						
E11	**VSS_E11**	Power	Ground						
E12	**DDR_ADDR_13**	DDR	SSTL						
E13	**DDR_ADDR_1**	DDR	SSTL						
E14	**DDR_ADDR_5**	DDR	SSTL						
E15	**DDR_ADDR_2**	DDR	SSTL						
E16	**DDR_ADDR_11**	DDR	SSTL						
F1	**DAC_RSET**	DAC	Analog						
F2	**DAC_COMP**	DAC	Analog						
F3	**GPIO_2**	GPIO	CMOS	ehci_ app_prt_ ovcurr1	uart_ahb_tx	ssis_rxd	sc_c1		2
F4	**VDD_F4**	Power	Digital Supply						
F5	**VSS_F5**	Power	Ground						
F6	**VSS_F6**	Power	Ground						
F7	**VSS_F7**	Power	Ground						
F8	**VSS_F8**	Power	Ground						
F9	**VSS_F9**	Power	Ground						
F10	**VSS_F10**	Power	Ground						
F11	**VSS_F11**	Power	Ground						
F12	**VDD_F12**	Power	Digital Supply						
F13	**DDR_ADDR_10**	DDR	SSTL						
F14	**DDR_ADDR_12**	DDR	SSTL						
F15	**DDR_ADDR_3**	DDR	SSTL						
F16	**DDR_BA_1**	DDR	SSTL						
G1	**VDDA_G1**	Power	Analog Supply						
G2	**GPIO_4**	GPIO	CMOS	ehci_prt_ pwr_1	uart_ahb_ rts_n	ssis_en	sc_c3		4
G3	**VDD_G3**	Power	Digital Supply						
G4	**VDD_G4**	Power	Digital Supply						
G5	**VSS_G5**	Power	Ground						
G6	**VSS_G6**	Power	Ground						
G7	**VSS_G7**	Power	Ground						
G8	**VSS_G8**	Power	Ground						
G9	**VSS_G9**	Power	Ground						
G10	**VSS_G10**	Power	Ground						
G11	**VSS_G11**	Power	Ground						
G12	**VDD_G12**	Power	Digital Supply						
G13	**DDR_RAS**	DDR	SSTL						
G14	**DDR_ADDR_0**	DDR	SSTL						
G15	**DDR_BA_0**	DDR	SSTL						
G16	**DDR_BA_2**	DDR	SSTL						

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
H1	**VDDA**	Power	Analog Supply						
H2	**CLK_AU**	GPIO	CMOS						45
H3	**VDD_H3**	Power	Digital Supply						
H4	**VDD_H4**	Power	Digital Supply						
H5	**VSS_H5**	Power	Ground						
H6	**VSS_H6**	Power	Ground						
H7	**VSS_H7**	Power	Ground						
H8	**VSS_H8**	Power	Ground						
H9	**VSS_H9**	Power	Ground						
H10	**VSS_H10**	Power	Ground						
H11	**VSS_H11**	Power	Ground						
H12	**VDD_H12**	Power	Digital Supply						
H13	**SMIO_20**	SMIO	CMOS		sd_d[2]				75
H14	**DDR_WE**	DDR	SSTL						
H15	**DDR_ODT**	DDR	SSTL						
H16	**DDR_CAS**	DDR	SSTL						
J1	**CLK_SI**	Sensor	CMOS						
J2	**XOUT**	Global	XOSC						
J3	**VDD_J3**	Power	Digital Supply						
J4	**VDD_J4**	Power	Digital Supply						
J5	**VDD_J5**	Power	Digital Supply						
J6	**VDD_J6**	Power	Digital Supply						
J7	**VDD_J7**	Power	Digital Supply						
J8	**SPCLK_ LVDS_P_1**	Sensor	SLVS / LVCMOS/ MIPI						
J9	**SPCLK_ LVDS_N_1**	Sensor	SLVS / LVCMOS/ MIPI						
J10	**VSS_J10**	Power	Ground						
J11	**VSS_J11**	Power	Ground						
J12	**VDD_J12**	Power	Digital Supply						
J13	**SMIO_2**	SMIO	CMOS		sd_clk				57
J14	**DDR_CKE**	DDR	SSTL						
J15	**DDR_RESET**	DDR	SSTL						
J16	**FSOURCE_0**	Global	Supply/ Ground						
K1	**XIN**	Global	XOSC						
K2	**RESERVED**								

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
K3	**TIMER1**	GPIO	CMOS	tm12_clk		idsp_pip_io-pad_mas-ter_hsync	enet_mdc		25
K4	**TIMER0**	GPIO	CMOS	tm11_clk			enet_2nd_ ref_clk		24
K5	**VDD33_K5**	Power	Digital Supply						
K6	**VDD33_K6**	Power	Digital Supply						
K7	**VDD33_K7**	Power	Digital Supply						
K8	**VDD33_K8**	Power	Digital Supply						
K9	**VDD33_K9**	Power	Digital Supply						
K10	**SMIO_21**	SMIO	CMOS		sd_d[3]				76
K11	**VDD_K11**	Power	Digital Supply						
K12	**VDD_K12**	Power	Digital Supply						
K13	**NAND_VDDO_ K13**	Power	Digital Supply						
K14	**NAND_VDDO_ K14**	Power	Digital Supply						
K15	**SMIO_19**	SMIO	CMOS		sd_d[1]				74
K16	**SMIO_3**	SMIO	CMOS		sd_cmd				58
L1	**SSI0EN1**	GPIO	CMOS	ssio_en1	norspi_en[1]				38
L2	**I2S_CLK**	I2S	CMOS	i2s_clk					41
L3	**I2S_SO**	I2S	CMOS	i2s_so					43
L4	**TIMER2**	GPIO	CMOS	tm13_clk	ssi0_en3	idsp_pip_io-pad_mas-ter_vsync	enet_mdio		26
L5	**VDD18_L5**	Power	Digital Supply						
L6	**VDD18_L6**	Power	Digital Supply						
L7	**VDD18_L7**	Power	Digital Supply						
L8	**VDD18_L8**	Power	Digital Supply						
L9	**VD0_OUT_4**	VOUT	CMOS	vd0_ out[4]					97
L10	**SVSYNC**	Sensor	CMOS	vin_ svsync	idsp_pip_io-pad_mas-ter_hsync				91
L11	**TEST_MODE**	Global	CMOS						
L12	**SMIO_5**	SMIO	CMOS		sd_wp				60
L13	**SMIO_10**	SMIO	CMOS		nand_d[1]	norspi_en[1]			65
L14	**SMIO_11**	SMIO	CMOS		nand_d[2]	norspi_en[2]			66
L15	**SMIO_9**	SMIO	CMOS		nand_d[0]	norspi_en[0]			64

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
L16	**SMIO_18**	SMIO	CMOS		sd_d[0]				73
M1	**SSI0MISO**	GPIO	CMOS	ssi0_rxd	norspi_dq[1]	uart_ahb_cts_n	ssis_txd		36
M2	**SSI0EN0**	GPIO	CMOS	ssi0_en0	norspi_en[0]	uart_ahb_rts_n	ssis_en		37
M3	**SSI0CLK**	GPIO	CMOS	ssi0_sclk	norspi_clk	uart_ahb_rx	ssis_sclk		34
M4	**I2S_SI**	I2S	CMOS	i2s_si					42
M5	**I2S_WS**	I2S	CMOS	i2s_ws					44
M6	**POR_L**	Global	CMOS						
M7	**ENET_TXD_1**	ENET	CMOS	enet_txd_1	sc_a2	enet_txd_1	ssi1_rxd	norspi_dq[1]	48
M8	**ENET_TXEN**	ENET	CMOS	enet_txen	sc_a0	enet_txen	ssi1_sclk	norspi_clk	46
M9	**VD0_OUT_13**	VOUT	CMOS	vd0_out[13]					106
M10	**VD_PWM**	GPIO	CMOS	pwm_0					113
M11	**VD0_CLK**	VOUT	CMOS	vd0_clk					109
M12	**SMIO_4**	SMIO	CMOS		sd_cd				59
M13	**SMIO_0**	SMIO	CMOS		nand_ce	norspi_clk			55
M14	**SMIO_6**	SMIO	CMOS		nand_re	norspi_dq[5]			61
M15	**SMIO_8**	SMIO	CMOS		nand_ale	norspi_dq[7]			63
M16	**SMIO_16**	SMIO	CMOS		nand_d[7]	norspi_dq[3]			71
N1	**SSI0MOSI**	GPIO	CMOS	ssi0_txd	norspi_dq[0]	uart_ahb_tx	ssis_rxd		35
N2	**IDCDATA**	IDC	CMOS	idc0data					28
N3	**IDC3CLK**	IDC	CMOS	idc2clk		vin_strig0			31
N4	**IDC3DATA**	IDC	CMOS	idc2data	vin_strig1				32
N5	**UART0RX**	GPIO	CMOS	uart0rx	uart_ahb_rx				39
N6	**IR_IN**	IR	CMOS	ir_in					33
N7	**SD_LVDS_P_7**	Sensor	SLVS / LVCMOS/ MIPI						
N8	**SD_LVDS_P_4**	Sensor	SLVS / LVCMOS/ MIPI						
N9	**VD0_VSYNC**	VOUT	CMOS	vd0_vsync					110
N10	**SHSYNC**	Sensor	CMOS	vin_shsync	idsp_pip_io-pad_mas-ter_vsync				92
N11	**VD0_OUT_12**	VOUT	CMOS	vd0_out[12]					105
N12	**VD0_OUT_14**	VOUT	CMOS	vd0_out[14]					107
N13	**VD0_OUT_15**	VOUT	CMOS	vd0_out[15]					108
N14	**SMIO_17**	SMIO	CMOS		nand_cle				72
N15	**SMIO_7**	SMIO	CMOS		nand_we	norspi_dq[6]			62
N16	**SMIO_1**	SMIO	CMOS		nand_rb	norspi_dq[4]			56
P1	**USB0_REXT**	USB	Analog						
P2	**SD_LVDS_P_3**	Sensor	SLVS / LVCMOS/ MIPI						
P3	**UART0TX**	GPIO	CMOS	uart0tx	uart_ahb_tx				40

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
P4	**WP**	GPIO	CMOS		nand_wp				54
P5	**SD_LVDS_N_1**	Sensor	SLVS / LVCMOS/ MIPI						
P6	**DETECT_VBUS**	USB	CMOS						
P7	**SD_LVDS_N_7**	Sensor	SLVS / LVCMOS/ MIPI						
P8	**SD_LVDS_N_4**	Sensor	SLVS / LVCMOS/ MIPI						
P9	**ENET_CRS_DV**	ENET	CMOS	enet_crs_ dv	sc_b2	enet_crs_dv	ssi1_en3	norspi_dq[2]	52
P10	**VD0_OUT_3**	VOUT	CMOS	vd0_ out[3]					96
P11	**VD0_OUT_1**	VOUT	CMOS	vd0_ out[1]					94
P12	**VD0_OUT_10**	VOUT	CMOS	vd0_ out[10]					103
P13	**VD0_OUT_11**	VOUT	CMOS	vd0_ out[11]					104
P14	**VD0_HVLD**	VOUT	CMOS	vd0_hvld					112
P15	**SMIO_15**	SMIO	CMOS		nand_d[6]	norspi_dq[2]			70
P16	**SMIO_12**	SMIO	CMOS		nand_d[3]	norspi_en[3]			67
R1	**USB0_DP**	USB	Analog						
R2	**SD_LVDS_N_3**	Sensor	SLVS / LVCMOS/ MIPI						
R3	**SD_LVDS_P_2**	Sensor	SLVS / LVCMOS/ MIPI						
R4	**SD_LVDS_P_0**	Sensor	SLVS / LVCMOS/ MIPI						
R5	**SD_LVDS_P_1**	Sensor	SLVS / LVCMOS/ MIPI						
R6	**IDCCLK**	IDC	CMOS	idc0_clk					27
R7	**SD_LVDS_P_6**	Sensor	SLVS / LVCMOS/ MIPI						
R8	**SD_LVDS_N_6**	Sensor	SLVS / LVCMOS/ MIPI						
R9	**ENET_RXD_0**	ENET	CMOS	enet_ rxd_0	sc_a3	enet_rxd_0	ssi1_en0	norspi_en[0]	49
R10	**ENET_RXD_1**	ENET	CMOS	enet_ rxd_1	sc_b0	enet_rxd_1	ssi1_en1	norspi_en[1]	50
R11	**VD0_OUT_2**	VOUT	CMOS	vd0_ out[2]					95
R12	**VD0_OUT_8**	VOUT	CMOS	vd0_ out[8]					101
R13	**VD0_OUT_5**	VOUT	CMOS	vd0_ out[5]					98
R14	**VD0_OUT_9**	VOUT	CMOS	vd0_ out[9]					102

Loc.	Pin Name	Group	Type	Multiplexed Functions					
				First	Second	Third	Fourth	Fifth	GPIO
R15	**SMIO_14**	SMIO	CMOS		nand_d[5]	norspi_dq[1]			69
R16	**SMIO_13**	SMIO	CMOS		nand_d[4]	norspi_dq[0]			68
T1	**USB0_DM**	USB	Analog						
T2	**VDDA33_T2**	Power	Analog Supply						
T3	**SD_LVDS_N_2**	Sensor	SLVS / LVCMOS/ MIPI						
T4	**SD_LVDS_N_0**	Sensor	SLVS / LVCMOS/ MIPI						
T5	**SPCLK_ LVDS_P_0**	Sensor	SLVS / LVCMOS/ MIPI						
T6	**SPCLK_ LVDS_N_0**	Sensor	SLVS / LVCMOS/ MIPI						
T7	**SD_LVDS_P_5**	Sensor	SLVS / LVCMOS/ MIPI						
T8	**SD_LVDS_N_5**	Sensor	SLVS / LVCMOS/ MIPI						
T9	**MIPI_VDDIO**	Power	Digital Supply						
T10	**ENET_REF_CLK**	ENET	CMOS	enet_ref_ clk	sc_b3	enet_rx_clk		norspi_dq[3]	53
T11	**ENET_TXD_0**	ENET	CMOS	enet_ txd_0	sc_a1	enet_txd_0	ssi1_txd	norspi_dq[0]	47
T12	**ENET_RX_ER**	ENET	CMOS	enet_rxer	sc_b1	enet_rxer	ssi1_en2	norspi_en[2]	51
T13	**VD0_HSYNC**	VOUT	CMOS	vd0_ hsync					111
T14	**VD0_OUT_7**	VOUT	CMOS	vd0_ out[7]					100
T15	**VD0_OUT_0**	VOUT	CMOS	vd0_ out[0]					93
T16	**VD0_OUT_6**	VOUT	CMOS	vd0_ out[6]					99

Table 7-1. Pin List and Mapping Table for the S2L55m Chip.

8. ADDITIONAL RESOURCES

Other Ambarella documents of potential interest include:

- *S2L Hardware Programming Reference Manual*
- *S2L RM: System Hardware*
- *S2L RM: Firmware and System Boot*
- *S2L Flexible Linux SDK: Release Notes*
- *S2L Flexible Linux EVK: Getting Started Guide*
- *S2L Flexible Linux EVK: Unit Test Program User Guide*
- *S2L Flexible Linux SDK: Code Development and Debug Environment*
- *S2L Flexible Linux SDK: SDK Specification and User Guide*
- *S2L Flexible Linux SDK Design Guide: Video Software*
- *S2L Flexible Linux SDK: Image Library API*
- *S2L Flexible Linux SDK Design Guide: Image Process*

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10. TYPOGRAPHICAL CONVENTIONS

This document provides technical detail using a set of consistent typographical conventions to help the user differentiate key concepts at a glance. Conventions include:

Example	Description
AmbaGuiGen, **DirectUSB** **Save, File > Save** **Power, Reset**, **Home**	Software names GUI commands and command sequences Computer / Hardware buttons
Flash_IO_control **da**, **status**, **enable**	Register names and register fields. For example, **Flash_IO_control** is the register for global control of Flash I/O, and bit 17 (**da)** is used for DMA acknowledgement.
GPIO81, **CLK_AU**	Hardware external pins
VIL, VIH, VOL, VOH	Hardware pin parameters
INT_O, RXDATA_I	Hardware pin signals
amb_performance_t **amb_operating_mode_t** **amb_set_operating_mode()**	API details (e.g., functions, structures, and type definitions)
`/usr/local/bin` `success = amb_set_operating_mode (amb_hal_base_address, & operating_mode)`	User entries into software dialogues and GUI windows File names and paths Command line scripting and Code

Table 10-1. Typographical Conventions for Technical Documents.

Additional Ambarella typographical conventions include:

- Acronyms are given in UPPER CASE using the default font (e.g., AHB, ARM11 and DDRIO).
- Names of Ambarella documents and publicly available standards, specifications, and databooks appear in *italic* type.

11. REVISION HISTORY

NOTE: Page/chapter numbers for previous drafts may differ from those in the current version.

Version	Date	Comments
0.1	8 April 2014	New S2L Part
0.2	30 June 2014	Correct typo regarding parallel input support (from 8-bit to 14-bit)
0.3	27 October 2014	Modify operating temperature range; Update maximum DDR size; update UART interface description

Table 11-1. Revision History.